

Product Name: ZX182S FMC Vita 57.1 Agilent Samtec probe E5379A test board - breakout adapter – passive FPGA Mezzanine Card
Agilent Probes: E5378A E5379A E5385A

Product Description: FPGA Mezzanine card , FMC , passive breakout adapter, meeting VITA 57.1 standard bus interfacing with Agilent Samtec differential / single ended probes Includes 10 rows x 40 pins, totaling **400** pins High Pin Count, HPC, (**200** pins for LPC – Low Pin Count), FCI Meg-Array, housing both CC (Carrier Card - Host) and MC (Mezzanine Card) connectors.

ZX182S is offered in HPC, LPC and FCI Meg-Array connector configuration, see ordering information

Fully compatible with 10 rows x 40 pins single ended or differential pairs design configuration

- All signals are accessible via designated probe's connector, IPEX, Header, and 0402 SMD package.
- All Clocks are accessible via IPEX-37 connectors
- JTAG signals accessible via 2x4 pin header
- All Power Supply signals accessible via 2x4 pin headers with on-board LEDs indicators.
- Improved signal integrity and crosstalk with **12 layers PCB** with each layers guarded by GROUND plane.
- Designed for **50Ω** single ended and **100Ω** differential trace impedance exceeding VITA 57.1 standard.
- DC to 10GHz bandwidth applications

GND test point for easy access as well as applying external ground reference

Application: FMC VITA 57.1 daughter card Bringup, testing, emulation, Xilinx development Virtex 6 Virtex 7 interface testing daughter board to host, modular design evaluations

Access: 2x4 pin header, SMD 0402 Package footprint as well as P68xx designated connectors

Pitch: 1.27mm (0.05") High Speed connector

Mates with : Xilinx FPGA development systems Virtex 6 Virtex 7 connecting daughter board to Host Any and all FMC VITA 57.1 compliant design CC-LPC-xxx CC-HPC-xxx MC-HPC-xxx MC-LPC-xxx where xxx is 10L, 10, 8.5L 8.5

Samtec Molex HI-SPEED HI-DENSITY SEARRAY design connectors.
 SEAM SADL SEAMP SEAR SEAMI SEAC FMC HPC LCP
 SEAF-040-08.0-L-10-2-A SEAF-040-08-L-10-2-A
 SEAFP-40 SEAMP-040 SEAMI-040 SEAR-040-10-10- SEAM-040
 All listed Samtec Molex FMC connectors listed, table below:

ZX18x FMC breakout adapter mates with the following Samtec Molex CC / MC SEARAY™ VITA 57.1 Connectors

Molex PN	Samtec PN	VITA PN	Description	Mated Stack Height
45971-4307	ASP-127796-01*	CC-LPC-10L	female	
45971-4317	ASP-134485-01*	CC-HPC-10L	female	
45971-4315	ASP-134486-01	CC-HPC-10	female	
45971-4305	ASP-134603-01	CC-LPC-10	female	
45970-4117	ASP-134601-01*	MC-HPC-8.5L	male	8.5 mm
45970-4115	ASP-134602-01	MC-HPC-8.5	male	8.5 mm
45970-4107	ASP-134605-01*	MC-LPC-8.5L	male	8.5 mm
45970-4105	ASP-134606-01	MC-LPC-8.5	male	8.5 mm
45970-4307	ASP-127797-01	MC-LPC-10L	male	10 mm
45970-4317	ASP-134487-01	MC-HPC-10L	male	10 mm
45970-4315	ASP-134488-01	MC-HPC-10	male	10 mm
45970-4305	ASP-134604-01	MC-LPC-10	male	10 mm

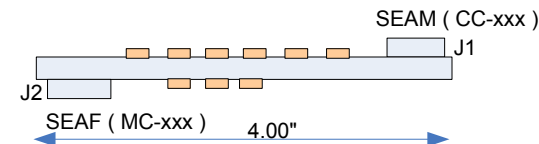
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ZX182S Block diagram, See Page 2

ZX182S , Passive FMC VITAL 57.1 breakout adapter – test board



CC: Carrier Card typically located on Host
 MC: Mezzanine Card, typically located on Mezzanine Card
 SEAF: SEARRAY Female connector
 SEAM: SEARRAY Plug (Male) connector

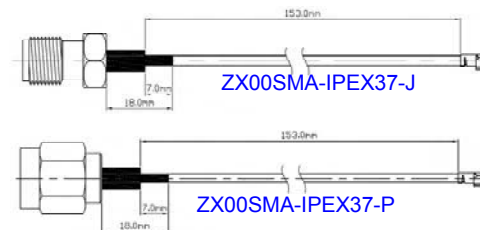
Probe connector, headers, IPEX-37 access points

ZX182S-X-X Package includes:

Part number	Quantity	Description
ZX182S-X-X	1	FMC Mezzanine Module
ZX00SMA-IPEX37-X	4	SMA to IPEX-37 cable assembly , Note 1, See ordering information

Notes:

1- Used for measuring or supplying external Clocks.



ZX182S-F-X Mates with any and all FMC VITA 57.1 compliant design using FCI Meg-Array 400 pins design. Meg-Array 10 rows x 40 pins FPGA Mezzanine Card (daughter)

Mated Stack Height: 4mm 6mm 8mm 10mm 12mm 14mm
 Meets Telcordia GR-1217-CORE and NPS25298-2 Specifications

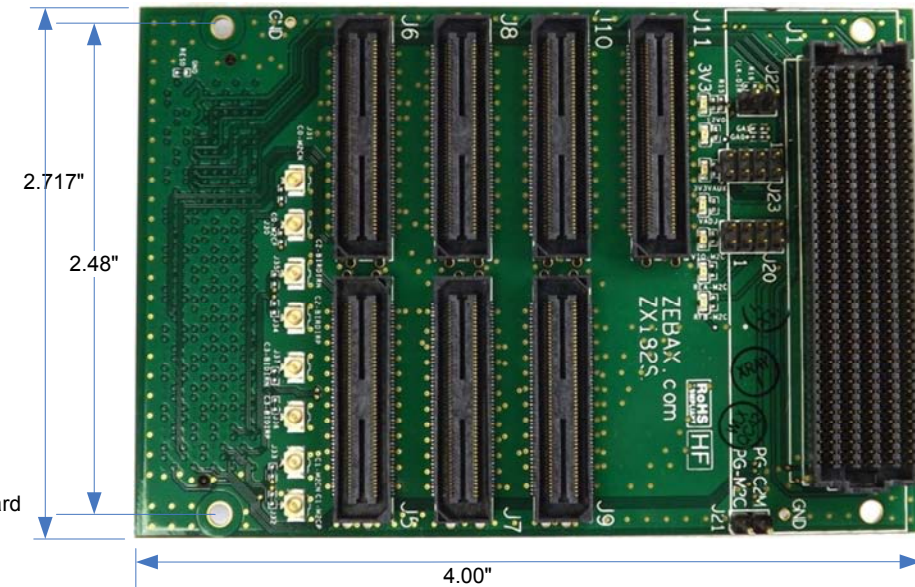
FCI ZX18x-F-X FCI Meg-Array 10rows x 40 pins FMC breakout adapter mates with the following FCI Meg-Array VITA 57.1 Connectors

Plug (CC)		Receptacle (MC)		
84520-002LF	84740-002LF	74221-001LF	74388-001LF	74390-001LF*
84520-101LF	84740-102LF	74221-101LF	74388-101LF	74390-101LF
84520-202LF*	84740-202LF	74221-201LF	74388-201LF	74390-201LF
84520-092LF	84740-092LF	74221-091LF	74388-091LF	74390-091LF
84520-192LF	84740-192LF	74221-191LF	74388-191LF	74390-191LF
84520-292LF	84740-292LF	74221-291LF	74388-291LF	74390-201LF
6mm Plug	0mm Plug	4mm	6mm	8mm

Mated Stack Height

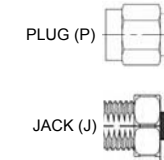
* Used on ZX182P-F-X

LF : Lead Free



Ordering INFO:

Part Number	options
ZX182S-X-X	J : SMA Jack (Standard) P : SMA Plug connector
	H : HPC - High Pin Count connector L : LPC - Low Pin Count connector F : FCI - FCI Meg-Array connector



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ASSEMBLY DRAWING

ITEM: ZX182S

DESCRIPTION: FMC VITA 57.1 test board for E5379A Agilent probe – passive mezzanine HPC LPC Meg-Array

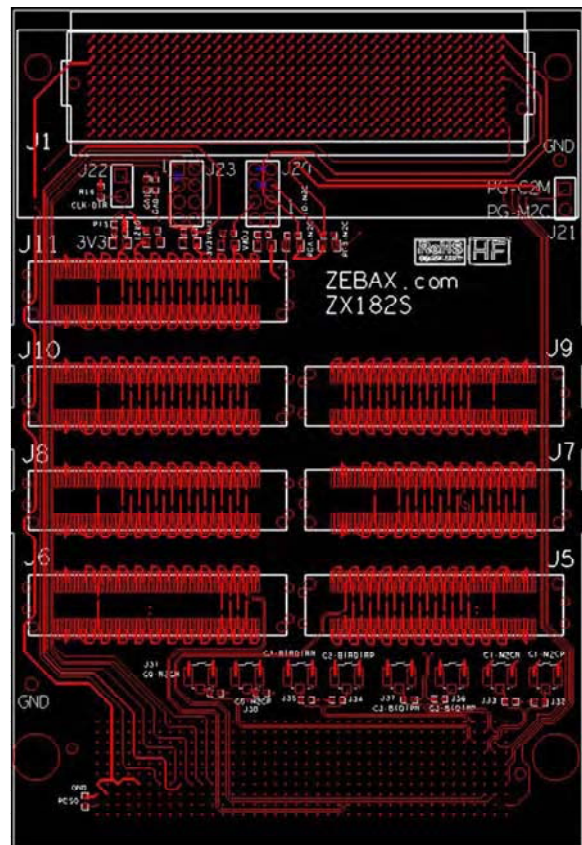
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DRAWN: SLAVIK

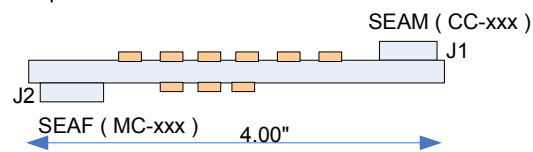
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SHEET: 1 OF 3

Product Name: ZX182S FMC Vita 57.1 Agilent Samtec porbe E5379A test board - breakout adapter – passive FPGA Mezzanine Card



ZX182S , Passive FMC VITAL 57.1 breakout adapter – test board



CC: Carrier Card typically located on Host
 MC: Mezzanine Card, typically located on Mezzanine Card
 SEAF: SEARRAY Female connector
 SEAM: SEARRAY Plug (Male) connector

Probe connector, headers, IPEX-37 access points

Typical SS signal connection using 0402 SMD Package



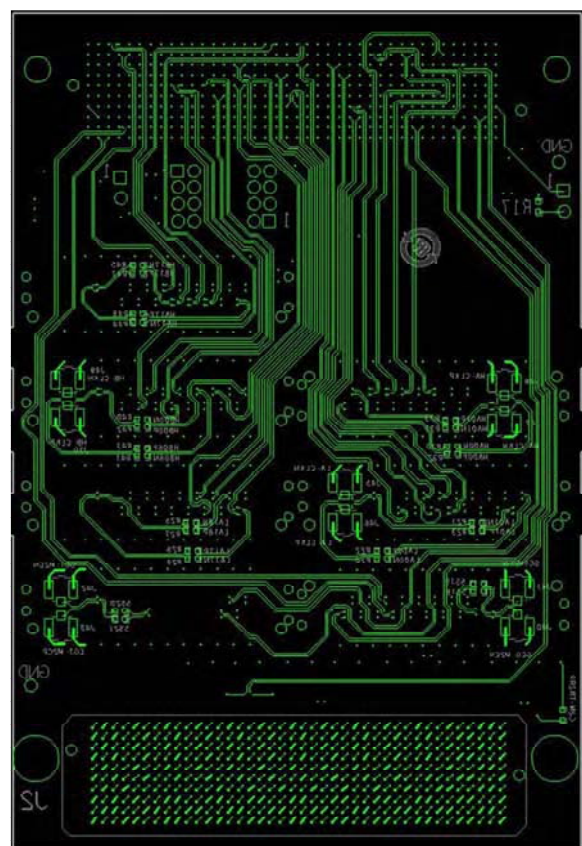
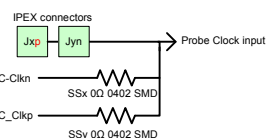
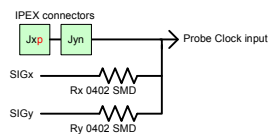
Break signal path:



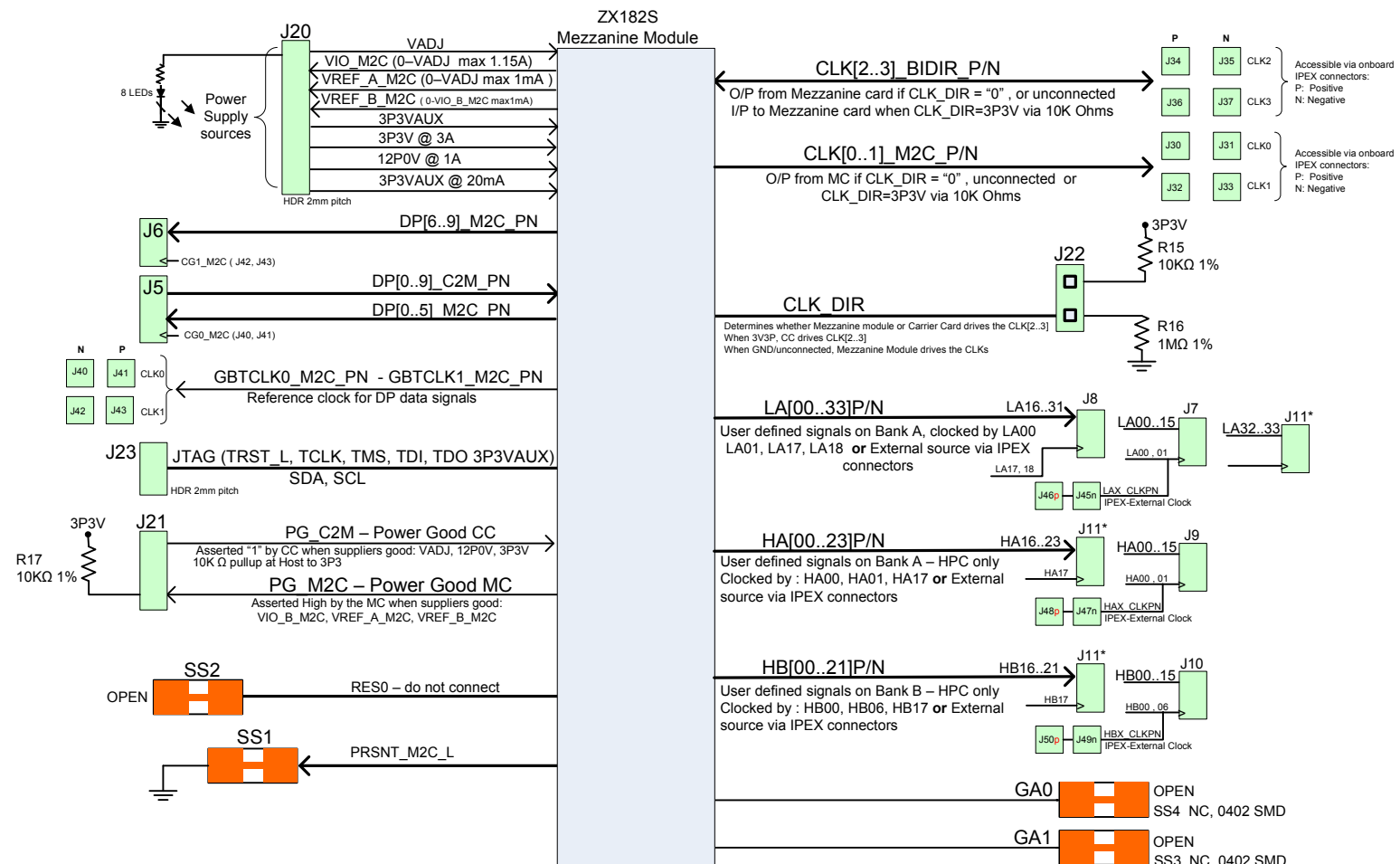
Clock routing technique

Probe clocks are routed using IPEX connectors for use with external clock sources as well as optional resistor stuffing as exhibited below. Jxp, Jxn are IPEX positive and negative IPEX connectors. The Rx, Ry (0402 SMD package) are not stuffed as default. SIGx, SIGy are defined signals reserved as probe clock option, if available. Please see Probe signal assignment table for assigned IPEX and availability of SIGx, SIGy per designed probe access.

MC clock source routing to probes are accessible at IPEX connectors. SS (0402 SMD package) can be used to disconnect MC from providing the Clock or install appropriate filtering, if applicable.



ZX132x (from Zebax) products complement ZX182S providing flying leads interface to any scope or Logic Analyzer.



- Note:**
- 1- MC Mezzanine Card - CC Carrier Card (Host)
 - 2- All Clocks are accessible via onboard IPEX connectors
 - 3- IPEX Jxp is shared terminal, Jxxn is shared terminal of the external clock source.
 - 4- J11* - J11 is shared connector supporting LA, HA, and HB signals. It has HA17 and HB17 clocking options

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	ITEM: ZX182S	
DESCRIPTION: FMC VITA 57.1 test board for E5379A Agilent probe – passive mezzanine HPC LPC Meg-Array		
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		SHEET: 2 OF 3

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Probe signal map: Below are signal and clock mapping for the designated probe connectors

J5					
Assigned	Pin	Signal	Signal	Pin	Assigned
GND	1	GND	GND	2	GND
NC	3	NC	NC	4	NC
GND	5	GND	GND	6	GND
DP0-C2M-N	7	D0-	D0+	8	DP0-C2M-P
GND	9	GND	GND	10	GND
DP1-C2M-N	11	D1-	D1+	12	DP1-C2M-P
GND	13	GND	GND	14	GND
DP2-C2M-N	15	D2-	D2+	16	DP2-C2M-P
GND	17	GND	GND	18	GND
DP3-C2M-N	19	D3-	D3+	20	DP3-C2M-P
GND	21	GND	GND	22	GND
DP4-C2M-N	23	D4-	D4+	24	DP4-C2M-P
GND	25	GND	GND	26	GND
DP5-C2M-N	27	D5-	D5+	28	DP5-C2M-P
GND	29	GND	GND	30	GND
DP6-C2M-N	31	D6-	D6+	32	DP6-C2M-P
GND	33	GND	GND	34	GND
DP7-C2M-N	35	D7-	D7+	36	DP7-C2M-P
GND	37	GND	GND	38	GND
DP8-C2M-N	39	D8-	D8+	40	DP8-C2M-P
GND	41	GND	GND	42	GND
DP9-C2M-N	43	D9-	D9+	44	DP9-C2M-P
GND	45	GND	GND	46	GND
DP0-M2C-N	47	D10-	D10+	48	DP0-M2C-P
GND	49	GND	GND	50	GND
DP1-M2C-N	51	D11-	D11+	52	DP1-M2C-P
GND	53	GND	GND	54	GND
DP2-M2C-N	55	D12-	D12+	56	DP2-M2C-P
GND	57	GND	GND	58	GND
DP3-M2C-N	59	D13-	D13+	60	DP3-M2C-P
GND	61	GND	GND	62	GND
DP4-M2C-N	63	D14-	D14+	64	DP4-M2C-P
GND	65	GND	GND	66	GND
DP5-M2C-N	67	D15-	D15+	68	DP5-M2C-P
GND	69	GND	GND	70	GND
NC	71	NC	NC	72	NC
GND	73	GND	GND	74	GND
NC	75	NC	NC	76	NC
GND	77	GND	GND	78	GND
GBTCLK0-M2C-N (J40-SS18)	79	D16-CLK-	D16-CLK+	80	GBTCLK0-M2C-P (J41-SS19)
GND	81	GND	GND	82	GND
NC	83	NC	NC	84	NC
GND	85	GND	GND	86	GND
NC	87	NC	NC	88	NC
NC	89	NC	NC	90	NC
NC	91	NC	NC	92	NC
GND	93	GND	GND	94	GND
GND	95	GND	GND	96	GND
NC	97	NC	NC	98	NC
NC	99	NC	NC	100	NC

J7					
Assigned	Pin	Signal	Signal	Pin	Assigned
GND	1	GND	GND	2	GND
NC	3	NC	NC	4	NC
GND	5	GND	GND	6	GND
LA00-N	7	D0-	D0+	8	LA00-P
GND	9	GND	GND	10	GND
LA01-N	11	D1-	D1+	12	LA01-P
GND	13	GND	GND	14	GND
LA02-N	15	D2-	D2+	16	LA02-P
GND	17	GND	GND	18	GND
LA03-N	19	D3-	D3+	20	LA03-P
GND	21	GND	GND	22	GND
LA04-N	23	D4-	D4+	24	LA04-P
GND	25	GND	GND	26	GND
LA05-N	27	D5-	D5+	28	LA05-P
GND	29	GND	GND	30	GND
LA06-N	31	D6-	D6+	32	LA06-P
GND	33	GND	GND	34	GND
LA07-N	35	D7-	D7+	36	LA07-P
GND	37	GND	GND	38	GND
LA08-N	39	D8-	D8+	40	LA08-P
GND	41	GND	GND	42	GND
LA09-N	43	D9-	D9+	44	LA09-P
GND	45	GND	GND	46	GND
LA10-N	47	D10-	D10+	48	LA10-P
GND	49	GND	GND	50	GND
LA11-N	51	D11-	D11+	52	LA11-P
GND	53	GND	GND	54	GND
LA12-N	55	D12-	D12+	56	LA12-P
GND	57	GND	GND	58	GND
LA13-N	59	D13-	D13+	60	LA13-P
GND	61	GND	GND	62	GND
LA14-N	63	D14-	D14+	64	LA14-P
GND	65	GND	GND	66	GND
LA15-N	67	D15-	D15+	68	LA15-P
GND	69	GND	GND	70	GND
NC	71	NC	NC	72	NC
GND	73	GND	GND	74	GND
NC	75	NC	NC	76	NC
GND	77	GND	GND	78	GND
XLA-CLKN - J45 (LA00-N (R20) LA01-N (R21))	79	D16-CLK-	D16-CLK+	80	XLA-CLKP - J46 (R22) LA00-P (R23) LA01-P (R23)
GND	81	GND	GND	82	GND
NC	83	NC	NC	84	NC
GND	85	GND	GND	86	GND
NC	87	NC	NC	88	NC
NC	89	NC	NC	90	NC
NC	91	NC	NC	92	NC
GND	93	GND	GND	94	GND
GND	95	GND	GND	96	GND
NC	97	NC	NC	98	NC
NC	99	NC	NC	100	NC

J9					
Assigned	Pin	Signal	Signal	Pin	Assigned
GND	1	GND	GND	2	GND
NC	3	NC	NC	4	NC
GND	5	GND	GND	6	GND
HA00-N	7	D0-	D0+	8	HA00-P
GND	9	GND	GND	10	GND
HA01-N	11	D1-	D1+	12	HA01-P
GND	13	GND	GND	14	GND
HA02-N	15	D2-	D2+	16	HA02-P
GND	17	GND	GND	18	GND
HA03-N	19	D3-	D3+	20	HA03-P
GND	21	GND	GND	22	GND
HA04-N	23	D4-	D4+	24	HA04-P
GND	25	GND	GND	26	GND
HA05-N	27	D5-	D5+	28	HA05-P
GND	29	GND	GND	30	GND
HA06-N	31	D6-	D6+	32	HA06-P
GND	33	GND	GND	34	GND
HA07-N	35	D7-	D7+	36	HA07-P
GND	37	GND	GND	38	GND
HA08-N	39	D8-	D8+	40	HA08-P
GND	41	GND	GND	42	GND
HA09-N	43	D9-	D9+	44	HA09-P
GND	45	GND	GND	46	GND
HA10-N	47	D10-	D10+	48	HA10-P
GND	49	GND	GND	50	GND
HA11-N	51	D11-	D11+	52	HA11-P
GND	53	GND	GND	54	GND
HA12-N	55	D12-	D12+	56	HA12-P
GND	57	GND	GND	58	GND
HA13-N	59	D13-	D13+	60	HA13-P
GND	61	GND	GND	62	GND
HA14-N	63	D14-	D14+	64	HA14-P
GND	65	GND	GND	66	GND
HA15-N	67	D15-	D15+	68	HA15-P
GND	69	GND	GND	70	GND
NC	71	NC	NC	72	NC
GND	73	GND	GND	74	GND
NC	75	NC	NC	76	NC
GND	77	GND	GND	78	GND
XHA-CLKN - J47 (HA00-N (R30) HA01-N (R31))	79	D16-CLK-	D16-CLK+	80	XHA-CLKP - J48 (R32) HA00-P (R33) HA01-P (R33)
GND	81	GND	GND	82	GND
NC	83	NC	NC	84	NC
GND	85	GND	GND	86	GND
NC	87	NC	NC	88	NC
NC	89	NC	NC	90	NC
NC	91	NC	NC	92	NC
GND	93	GND	GND	94	GND
GND	95	GND	GND	96	GND
NC	97	NC	NC	98	NC
NC	99	NC	NC	100	NC

J11					
Assigned	Pin	Signal	Signal	Pin	Assigned
GND	1	GND	GND	2	GND
NC	3	NC	NC	4	NC
GND	5	GND	GND	6	GND
HA16-N	7	D0-	D0+	8	HA16-P
GND	9	GND	GND	10	GND
HA17-N	11	D1-	D1+	12	HA17-P
GND	13	GND	GND	14	GND
HA18-N	15	D2-	D2+	16	HA18-P
GND	17	GND	GND	18	GND
HA19-N	19	D3-	D3+	20	HA19-P
GND	21	GND	GND	22	GND
HA20-N	23	D4-	D4+	24	HA20-P
GND	25	GND	GND	26	GND
HA21-N	27	D5-	D5+	28	HA21-P
GND	29	GND	GND	30	GND
HA22-N	31	D6-	D6+	32	HA22-P
GND	33	GND	GND	34	GND
HA23-N	35	D7-	D7+	36	HA23-P
GND	37	GND	GND	38	GND
HB16-N	39	D8-	D8+	40	HB16-P
GND	41	GND	GND	42	GND
HB17-N	43	D9-	D9+	44	HB17-P
GND	45	GND	GND	46	GND
HB18-N	47	D10-	D10+	48	HB18-P
GND	49	GND	GND	50	GND
HB19-N	51	D11-	D11+	52	HB19-P
GND	53	GND	GND	54	GND
HB20-N	55	D12-	D12+	56	HB20-P
GND	57	GND	GND	58	GND
HB21-N	59	D13-	D13+	60	HB21-P
GND	61	GND	GND	62	GND
LA32-N	63	D14-	D14+	64	LA32-P
GND	65	GND	GND	66	GND
LA33-N	67	D15-	D15+	68	LA33-P
GND	69	GND	GND	70	GND
NC	71	NC	NC	72	NC
GND	73	GND	GND	74	GND
NC	75	NC	NC	76	NC
GND	77	GND	GND	78	GND
HA17-N (R44) HB17-N (R45)	79	D16-CLK-	D16-CLK+	80	(R46) HA17-P (R47) HB17-P
GND	81	GND	GND	82	GND
NC	83	NC	NC	84	NC
GND	85	GND	GND	86	GND
NC	87	NC	NC	88	NC
NC	89	NC	NC	90	NC
NC	91	NC	NC	92	NC
GND	93	GND	GND	94	GND
GND	95	GND	GND	96	GND
NC	97	NC	NC	98	NC
NC	99	NC	NC	100	NC

Vita57.1 Power Supply rails			
Voltage supply	Voltage	Max. Current HPC (LPC)	Description
VADJ	0- 3.3V	4A (2A)	Adjustable supply voltage from CC to the IO MC module.
VIO-B-M2C	0 - VADJ	1.15 (NA)	Supplied voltage generated by MC powering the IO banks on the FPGA interfacing to the Bank B IO pins of the connector
VREF-A-M2C	0 - VADJ	1mA*	Reference voltage used by the bank A data pins, LAXx, HAXx. No Connect if Bank A reference voltage is not required.
VREF-B-M2C	0 - VIO-B-M2C	1mA (NA)*	Reference voltage used by the bank B data pins, HBxx. No Connect if Bank A reference voltage is not required.
3P3VAUX	3.3V	20mA*	Auxiliary power supply from CC to the IO MC module.
3P3	3.3V	3A	Power supply from CC to the IO MC module.
12P0V	12.0V	1A	Power supply from CC to the IO MC module.

NA: Not available for LPC connector CC: Carrier Card (Host) MC: Mezzanine Card
 * Due to supply rail's max. current limitation, the onboard LED indicator is populated but the current limiting resistor is NOT populated.

J20			
Assigned	Pin	Pin	Assigned
VIO-B-M2C	1	2	3P3
VREF-A-M2C	3	4	VADJ
VREF-B-M2C	5	6	3P3VAUX
GND	7	8	12P0V

J23			
Assigned	Pin	Pin	Assigned
TDI	1	2	TD0
3P3VAUX	3	4	TCK
I2C-SCL	5	6	TRST-L
I2C-SDA	7	8	TMS

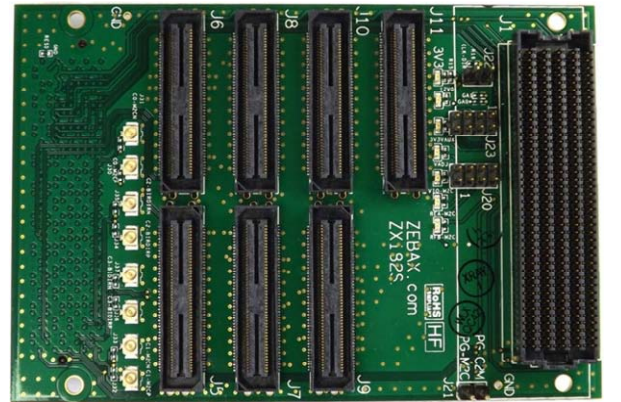
J21			
Assigned	Pin	Pin	Assigned
PG-C2M	1	2	PG-M2C*

* 10K Ω (R17) pullup resistor to 3P3 supply rail

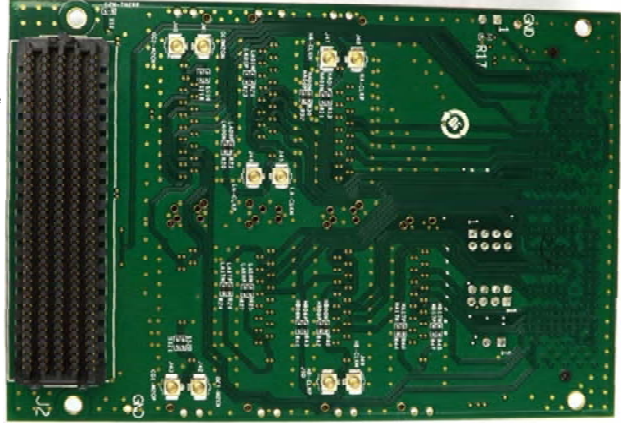
J22			
Assigned	Pin	Pin	Assigned
CLK-DIR*	1	2	GND**

* 10K Ω Pullup resistor R15 to 3P3 supply rail
 ** 1M K Ω Pulldown resistor R16 to GND

ZX182S Top



ZX182S Bottom



Note
 ALL ZEBAX products are RoHS compliant and Lead Free unless otherwise indicated.

J6					
Assigned	Pin	Signal	Signal	Pin	Assigned
GND	1	GND	GND	2	GND
NC	3	NC	NC	4	NC
GND	5	GND	GND	6	GND
DP6-M2C-N	7	D0-	D0+	8	DP1-M2C-P
GND	9	GND	GND	10	GND
DP7-M2C-N	11	D1-	D1+	12	DP1-M2C-P
GND	13	GND	GND	14	GND
DP8-M2C-N	15	D2-	D2+	16	DP1-M2C-P
GND	17	GND	GND	18	GND
DP8-M2C-N	19	D3-	D3+	20	DP1-M2C-P
GND	21	GND	GND	22	GND
NC	23	D4-	D4+	24	NC
GND	25	GND	GND	26	GND
NC	27	D5-	D5+	28	NC
GND	29	GND	GND	30	GND
NC	31	D6-	D6+	32	NC
GND	33	GND	GND	34	GND
NC	35	D7-	D7+	36	NC
GND	37	GND	GND	38	GND</