Product Name: **ZX182P FMC Vita 57.1 Tektronix P68xx (6880) test board - breakout adapter – passive FPGA Mezzanine Card**

Product Description: FPGA Mezzanine card , FMC , passive breakout adapter, meeting VITA 57.1 standard bus interfacing with Tektronix P68xx (6880) differential / single ended signaling applications. Includes 10 rows x 40 pins, totaling **400** pins High Pin Count, HPC, (**200** pins for LPC – Low Pin Count), FCI Meg-Array, housing both CC (Carrier Card - Host) and MC (Mezzanine Card) connectors.

ZX182P is offered in HPC, LPC and FCI Meg-Array connector configuration, see ordering information

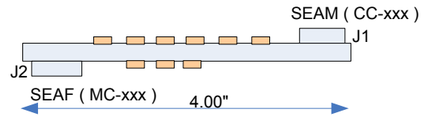
Fully compatible with 10 rows x 40 pins single ended or differential pairs design configuration

- **All** signals are accessible via designated P6880 connector, IPEX, Header, and 0402 SMD package.
- All Clocks are accessible via IPEX-37 connectors
- JTAG signals accessible via 2x4 pin header
- All Power Supply signals accessible via 2x4 pin headers with on-board LEDs indicators.
- Improved signal integrity and crosstalk with **12 layers PCB** with each layers guarded by GROUND plane.
- Designed for **50Ω** single ended and **100Ω** differential trace impedance exceeding VITA 57.1 standard.
- DC to 10GHz bandwidth applications

GND test point for easy access as well as applying external ground reference

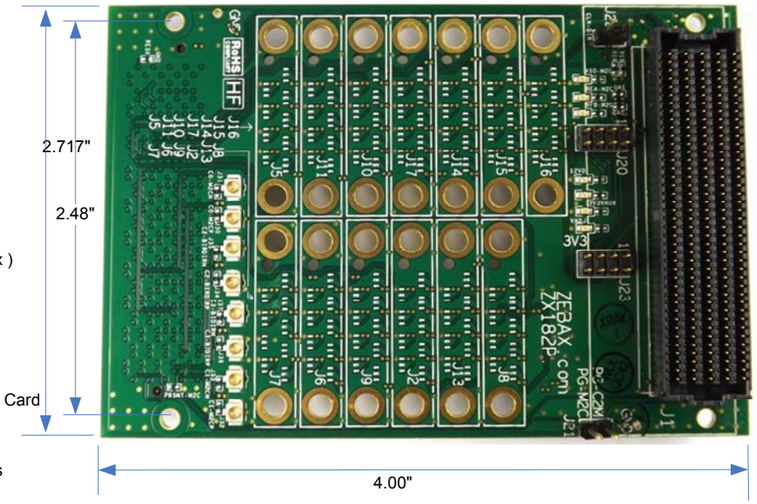
ZX182P Block diagram, See Page 2

ZX182P , Passive FMC VITAL 57.1 breakout adapter – test board



CC: Carrier Card typically located on Host
MC: Mezzanine Card, typically located on Mezzanine Card
SEAF: SEARRAY Female connector
SEAM: SEARRAY Plug (Male) connector

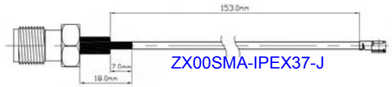
Probe connector, headers, IPEX-37 access points

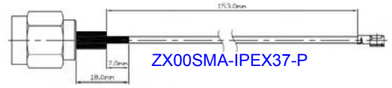


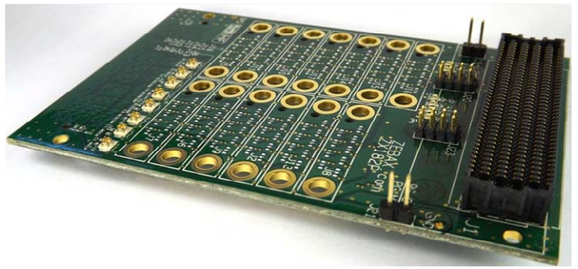
ZX182P-X-X Package includes:

Part number	Quantity	Description
ZX182P-X-X	1	FMC Mezzanine Module
ZX00SMA-IPEX37-X	4	SMA to IPEX-37 cable assembly , Note 1, See ordering information

Notes:
1- Used for measuring or supplying external Clocks.







ZX182P board thickness is 1.5mm +-10%

Application: FMC VITA 57.1 daughter card Bringup, testing, emulation, Xilinx development Virtex 6 Virtex 7 interface testing daughter board to host, modular design evaluations

Access: 2x4 pin header, SMD 0402 Package footprint as well as P68xx designated connectors

Pitch: 1.27mm (0.05") High Speed connector

Mates with : Xilinx FPGA development systems Virtex 6 Virtex 7 connecting daughter board to Host
Any and all FMC VITA 57.1 compliant design CC-LPC-xxx CC-HPC-xxx MC-HPC-xxx MC-LPC-xxx where xxx is 10L, 10, 8.5L 8.5
Samtec Molex HI-SPEED HI-DENSITY SEARRAY design connectors.
SEAM SADL SEAMP SEAR SEAMI SEAC FMC HPC LCP
SEAF-040-08.0-L-10-2-A SEAF-040-08-L-10-2-A
SEAFP-40 SEAMP-040 SEAMI-040 SEAR-040-10-10- SEAM-040
All listed Samtec Molex FMC connectors listed, table below:

ZX182P-F-X Mates with any and all FMC VITA 57.1 compliant design using FCI Meg-Array 400 pins design. Meg-Array 10 rows x 40 pins FPGA Mezzanine Card (daughter)

Mated Stack Height: 4mm 6mm 8mm 10mm 12mm 14mm
Meets Telcordia GR-1217-CORE and NPS25298-2 Specifications

ZX18x FMC breakout adapter mates with the following Samtec Molex CC / MC SEARAY™ VITA 57.1 Connectors

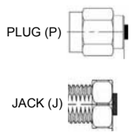
Molex PN	Samtec PN	VITA PN	Description	Mated Stack Height
45971-4307	ASP-127796-01*	CC-LPC-10L	female	
45971-4317	ASP-134485-01*	CC-HPC-10L	female	
45971-4315	ASP-134486-01	CC-HPC-10	female	
45971-4305	ASP-134603-01	CC-LPC-10	female	
45970-4117	ASP-134601-01*	MC-HPC-8.5L	male	8.5 mm
45970-4115	ASP-134602-01	MC-HPC-8.5	male	8.5 mm
45970-4107	ASP-134605-01*	MC-LPC-8.5L	male	8.5 mm
45970-4105	ASP-134606-01	MC-LPC-8.5	male	8.5 mm
45970-4307	ASP-127797-01	MC-LPC-10L	male	10 mm
45970-4317	ASP-134487-01	MC-HPC-10L	male	10 mm
45970-4315	ASP-134488-01	MC-HPC-10	male	10 mm
45970-4305	ASP-134604-01	MC-LPC-10	male	10 mm

ZX18x-F-X FCI Meg-Array 10rows x 40 pins FMC breakout adapter mates with the following FCI Meg-Array VITA 57.1 Connectors

Plug (CC)		Receptacle (MC)		
84520-002LF	84740-002LF	74221-001LF	74388-001LF	74390-001LF*
84520-101LF	84740-102LF	74221-101LF	74388-101LF	74390-101LF
84520-202LF*	84740-202LF	74221-201LF	74388-201LF	74390-201LF
84520-092LF	84740-092LF	74221-091LF	74388-091LF	74390-091LF
84520-192LF	84740-192LF	74221-191LF	74388-191LF	74390-191LF
84520-292LF	84740-292LF	74221-291LF	74388-291LF	74390-201LF
6mm Plug	0mm Plug	4mm	6mm	8mm
Mated Stack Height				

*** Used on ZX182P-F-X**
LF : Lead Free

Ordering INFO:
Part Number
ZX182P-X-X options



- J : SMA Jack (Standard)
- P: SMA Plug connector
- H : HPC - High Pin Count connector
- L : LPC - Low Pin Count connector
- F : FCI - FCI Meg-Array connector

Note
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SPECIFIED DIMENSIONS ARE INCHES (MM).
ROHS COMPLIANT

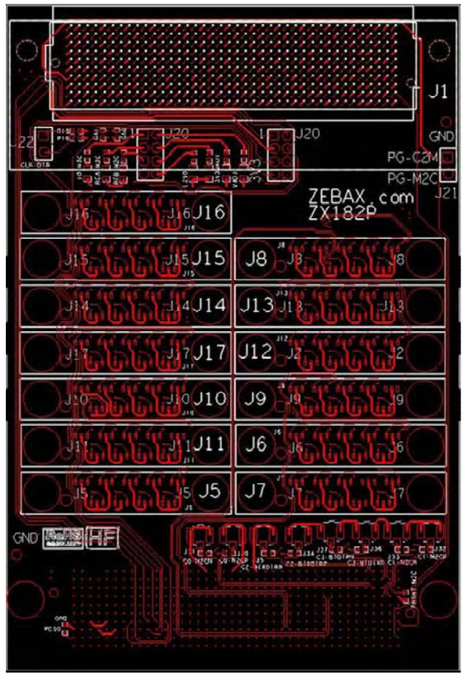
ASSEMBLY DRAWING

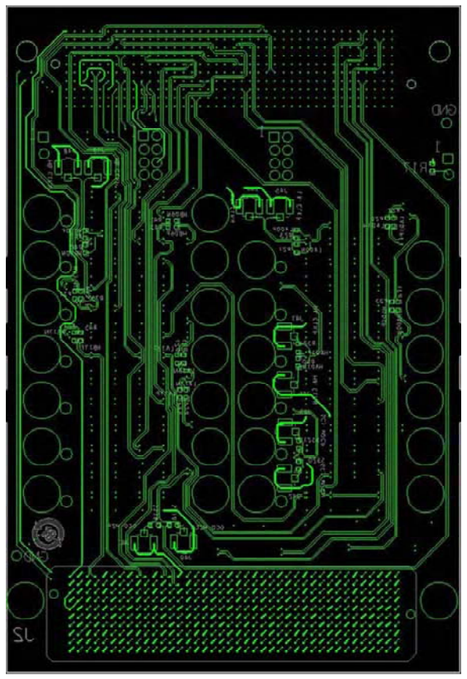
ITEM: ZX182P

DESCRIPTION: **FMC VITA 57.1 test board for P6880 Tektronix probe – passive mezzanine HPC LPC Meg-Array**

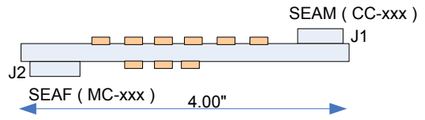
CHECKED:	DRAWN:	REVISSION: 1.0
M. MARINA	SLAVIK	SHEET: 1 OF 3

Product Name: **ZX182P FMC Vita 57.1 Tektronix P68xx (6880) test board - breakout adapter – passive FPGA Mezzanine Card**





ZX182P , Passive FMC VITAL 57.1 breakout adapter – test board



CC: Carrier Card typically located on Host
MC: Mezzanine Card, typically located on Mezzanine Card
SEAF: SEARRAY Female connector
SEAM: SEARRAY Plug (Male) connector

Probe connector, headers, IPEX-37 access points

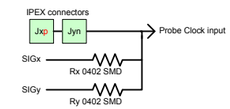
Typical SS signal connection using 0402 SMD Package

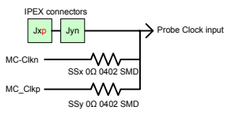
Break signal path:

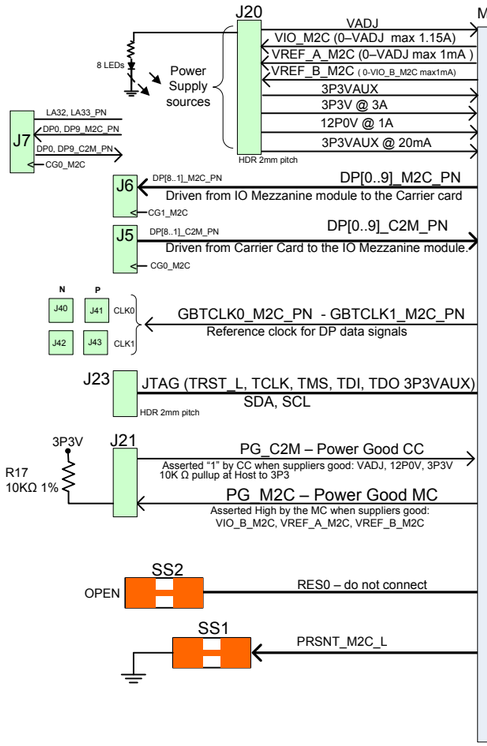
Clock routing technique

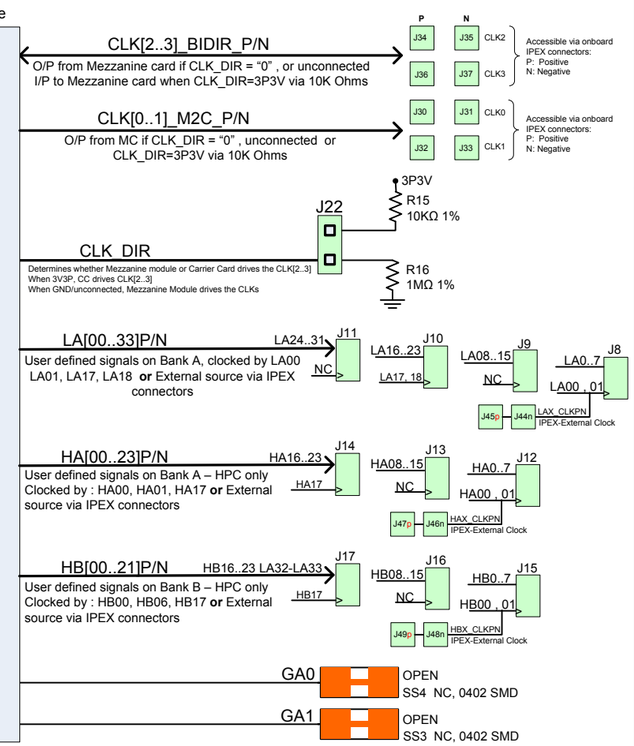
Probe clocks are routed using IPEX connectors for use with external clock sources as well as optional resistor stuffing as exhibited below. Jxp, Jxn are IPEX positive and negative IPEX connectors. The Rx, Ry (0402 SMD package) are not stuffed as default. SIGx, SIGy are defined signals reserved as probe clock option, if available. Please see Probe signal assignment table for assigned IPEX and availability of SIGx, SIGy per designed probe access.

MC clock source routing to probes are accessible at IPEX connectors. SS (0402 SMD package) can be used to disconnect MC from providing the Clock or install appropriate filtering, if applicable.







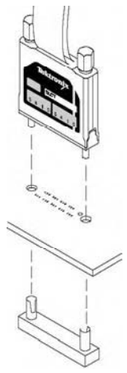


Note:
1- **MC** Mezzanine Card - **CC** Carrier Card (Host)
2- All Clocks are accessible via onboard IPEX connectors
3- IPEX Jxxp is positive terminal, Jxxn is negative terminal of the external clock source.

P6880 P68xx Probes

P68xx Logic Analyzer Probes connect TLA7Axx series Logic Analyzer module to target systems. P68xx probe connect to ZX182P (target) through podlets holders or leadsets.

Installation requirement : Probe installation requires **thin elastomer holder** with the **nut bar** for ZX182P



Note

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SPECIFIED DIMENSIONS ARE INCHES (MM).
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ASSEMBLY DRAWING

ITEM: ZX182P

DESCRIPTION: FMC VITA 57.1 test board for P6880 Tektronix probe – passive mezzanine HPC LPC Meg-Array

CHECKED: M. MARINA
DRAWN: SLAVIK
REVISSION: 1.0
SHEET: 2 OF 3

J2

Probe signal map: Below are signal and clock mapping for the designated probe connectors

J5

Assigned	Pin	Signal	Signal	Pin	Assigned
GBTCLK0-M2C-N (J40 - SS18)+	A15	CLK-			
GND	A14				
GBTCLK0-M2C-P (J41 - SS19)+	A13	CLK+			
DP7-C2M-N	A12	Data6-	Data7+	B12	DP8-C2M-P
GND	A11			B11	GND
DP7-C2M-P	A10	Data6+	Data7-	B10	DP8-C2M-N
DP5-C2M-N	A9	Data4-	Data5+	B9	DP6-C2M-P
GND	A8			B8	GND
DP5-C2M-P	A7	Data4+	Data5-	B7	DP6-C2M-N
DP3-C2M-N	A6	Data2-	Data3+	B6	DP4-C2M-P
GND	A5			B5	GND
DP3-C2M-P	A4	Data2+	Data3-	B4	DP4-C2M-N
DP1-C2M-N	A3	Data0-	Data1+	B3	DP2-C2M-P
GND	A2			B2	GND
DP1-C2M-P	A1	Data0+	Data1-	B1	DP2-C2M-N

J9

Assigned	Pin	Signal	Signal	Pin	Assigned
NC	A15	CLK-			
GND	A14				
NC	A13	CLK+			
LA14-N	A12	Data6-	Data7+	B12	LA15-P
GND	A11			B11	GND
LA14-P	A10	Data6+	Data7-	B10	LA15-N
LA12-N	A9	Data4-	Data5+	B9	LA13-P
GND	A8			B8	GND
LA12-P	A7	Data4+	Data5-	B7	LA13-N
LA10-N	A6	Data2-	Data3+	B6	LA11-P
GND	A5			B5	GND
LA10-P	A4	Data2+	Data3-	B4	LA11-N
LA08-N	A3	Data0-	Data1+	B3	LA09-P
GND	A2			B2	GND
LA08-P	A1	Data0+	Data1-	B1	LA09-N

J13

Assigned	Pin	Signal	Signal	Pin	Assigned
NC	A15	CLK-			
GND	A14				
NC	A13	CLK+			
HA14-N	A12	Data6-	Data7+	B12	HA15-P
GND	A11			B11	GND
HA14-P	A10	Data6+	Data7-	B10	HA15-N
HA12-N	A9	Data4-	Data5+	B9	HA13-P
GND	A8			B8	GND
HA12-P	A7	Data4+	Data5-	B7	HA13-N
HA10-N	A6	Data2-	Data3+	B6	HA11-P
GND	A5			B5	GND
HA10-P	A4	Data2+	Data3-	B4	HA11-N
HA08-N	A3	Data0-	Data1+	B3	HA09-P
GND	A2			B2	GND
HA08-P	A1	Data0+	Data1-	B1	HA09-N

J6

Assigned	Pin	Signal	Signal	Pin	Assigned
GBTCLK1-M2C-N (J42 - SS20)+	A15	CLK-			
GND	A14				
GBTCLK1-M2C-P (J43 - SS21)+	A13	CLK+			
DP7-M2C-N	A12	Data6-	Data7+	B12	DP8-M2C-P
GND	A11			B11	GND
DP7-M2C-P	A10	Data6+	Data7-	B10	DP8-M2C-N
DP5-M2C-N	A9	Data4-	Data5+	B9	DP6-M2C-P
GND	A8			B8	GND
DP5-M2C-P	A7	Data4+	Data5-	B7	DP6-M2C-N
DP3-M2C-N	A6	Data2-	Data3+	B6	DP4-M2C-P
GND	A5			B5	GND
DP3-M2C-P	A4	Data2+	Data3-	B4	DP4-M2C-N
DP1-M2C-N	A3	Data0-	Data1+	B3	DP2-M2C-P
GND	A2			B2	GND
DP1-M2C-P	A1	Data0+	Data1-	B1	DP2-M2C-N

J10

Assigned	Pin	Signal	Signal	Pin	Assigned
(LA17-N - R24) (LA18-N - R25)++	A15	CLK-			
GND	A14				
(LA17-P - R26) (LA18-P - R27)++	A13	CLK+			
LA22-N	A12	Data6-	Data7+	B12	LA23-P
GND	A11			B11	GND
LA22-P	A10	Data6+	Data7-	B10	LA23-N
LA20-N	A9	Data4-	Data5+	B9	LA21-P
GND	A8			B8	GND
LA20-P	A7	Data4+	Data5-	B7	LA21-N
LA18-N	A6	Data2-	Data3+	B6	LA19-P
GND	A5			B5	GND
LA18-P	A4	Data2+	Data3-	B4	LA19-N
LA16-N	A3	Data0-	Data1+	B3	LA17-P
GND	A2			B2	GND
LA16-P	A1	Data0+	Data1-	B1	LA17-N

J14

Assigned	Pin	Signal	Signal	Pin	Assigned
(HA17-N - R34)++	A15	CLK-			
GND	A14				
(HA17-P - R35)++	A13	CLK+			
HA22-N	A12	Data6-	Data7+	B12	HA23-P
GND	A11			B11	GND
HA22-P	A10	Data6+	Data7-	B10	HA23-N
HA20-N	A9	Data4-	Data5+	B9	HA21-P
GND	A8			B8	GND
HA20-P	A7	Data4+	Data5-	B7	HA21-N
HA18-N	A6	Data2-	Data3+	B6	HA19-P
GND	A5			B5	GND
HA18-P	A4	Data2+	Data3-	B4	HA19-N
HA16-N	A3	Data0-	Data1+	B3	HA17-P
GND	A2			B2	GND
HA16-P	A1	Data0+	Data1-	B1	HA17-N

J7

Assigned	Pin	Signal	Signal	Pin	Assigned
GBTCLK0-M2C-N (J40 - SS18)+	A15	CLK-			
GND	A14				
GBTCLK0-M2C-P (J41 - SS19)+	A13	CLK+			
NC	A12	Data6-	Data7+	B12	DP9-M2C-P
GND	A11			B11	GND
NC	A10	Data6+	Data7-	B10	DP9-M2C-N
DP0-M2C-N	A9	Data4-	Data5+	B9	NC
GND	A8			B8	GND
DP0-M2C-P	A7	Data4+	Data5-	B7	NC
LA33-N	A6	Data2-	Data3+	B6	DP9-C2M-P
GND	A5			B5	GND
LA33-P	A4	Data2+	Data3-	B4	DP9-C2M-N
DP0-C2M-N	A3	Data0-	Data1+	B3	LA32-P
GND	A2			B2	GND
DP0-C2M-P	A1	Data0+	Data1-	B1	LA32-N

J11

Assigned	Pin	Signal	Signal	Pin	Assigned
NC	A15	CLK-			
GND	A14				
NC	A13	CLK+			
LA30-N	A12	Data6-	Data7+	B12	LA31-P
GND	A11			B11	GND
LA30-P	A10	Data6+	Data7-	B10	LA31-N
LA28-N	A9	Data4-	Data5+	B9	LA29-P
GND	A8			B8	GND
LA28-P	A7	Data4+	Data5-	B7	LA29-N
LA26-N	A6	Data2-	Data3+	B6	LA27-P
GND	A5			B5	GND
LA26-P	A4	Data2+	Data3-	B4	LA27-N
LA24-N	A3	Data0-	Data1+	B3	LA25-P
GND	A2			B2	GND
LA24-P	A1	Data0+	Data1-	B1	LA25-N

J15

Assigned	Pin	Signal	Signal	Pin	Assigned
XHB-CLK-N - J48 (HB00-N - R40) (HB06-N - R41)++	A15	CLK-			
GND	A14				
XHB-CLK-P -J49 (HB00-P - R40) (HB06-P - R43)++	A13	CLK+			
HB06-N	A12	Data6-	Data7+	B12	HB07-P
GND	A11			B11	GND
HB06-P	A10	Data6+	Data7-	B10	HB07-N
HB04-N	A9	Data4-	Data5+	B9	HB05-P
GND	A8			B8	GND
HB04-P	A7	Data4+	Data5-	B7	HB05-N
HB02-N	A6	Data2-	Data3+	B6	HB03-P
GND	A5			B5	GND
HB02-P	A4	Data2+	Data3-	B4	HB03-N
HB00-N	A3	Data0-	Data1+	B3	HB01-P
GND	A2			B2	GND
HB00-P	A1	Data0+	Data1-	B1	HB01-N

J8

Assigned	Pin	Signal	Signal	Pin	Assigned
XLA-CLK-N - J44 (LA00-N - R21) (LA01-N - R20)++	A15	CLK-			
GND	A14				
XLA-CLK-P - J45 (LA00-P - R23) (LA01-P - R22)++	A13	CLK+			
LA06-N	A12	Data6-	Data7+	B12	LA07-P
GND	A11			B11	GND
LA06-P	A10	Data6+	Data7-	B10	LA07-N
LA04-N	A9	Data4-	Data5+	B9	LA05-P
GND	A8			B8	GND
LA04-P	A7	Data4+	Data5-	B7	LA05-N
LA02-N	A6	Data2-	Data3+	B6	LA03-P
GND	A5			B5	GND
LA02-P	A4	Data2+	Data3-	B4	LA03-N
LA00-N	A3	Data0-	Data1+	B3	LA01-P
GND	A2			B2	GND
LA00-P	A1	Data0+	Data1-	B1	LA01-N

J12

Assigned	Pin	Signal	Signal	Pin	Assigned
XHA-CLK-N - J46 (HA00-N - R31) (HA01-N - R30)++	A15	CLK-			
GND	A14				
XHA-CLK-P - J47 (HA00-P - R33) (HA01-P - R32)++	A13	CLK+			
HA06-N	A12	Data6-	Data7+	B12	HA07-P
GND	A11			B11	GND
HA06-P	A10	Data6+	Data7-	B10	HA07-N
HA04-N	A9	Data4-	Data5+	B9	HA05-P
GND	A8			B8	GND
HA04-P	A7	Data4+	Data5-	B7	HA05-N
HA02-N	A6	Data2-	Data3+	B6	HA03-P
GND	A5			B5	GND
HA02-P	A4	Data2+	Data3-	B4	HA03-N
HA00-N	A3	Data0-	Data1+	B3	HA01-P
GND	A2			B2	GND
HA00-P	A1	Data0+	Data1-	B1	HA01-N

J16

Assigned	Pin	Signal	Signal	Pin	Assigned
NC	A15	CLK-			
GND	A14				
NC	A13	CLK+			
HB14-N	A12	Data6-	Data7+	B12	HB15-P
GND	A11			B11	GND
HB14-P	A10	Data6+	Data7-	B10	HB15-N
HB12-N	A9	Data4-	Data5+	B9	HB13-P
GND	A8			B8	GND
HB12-P	A7	Data4+	Data5-	B7	HB13-N
HB10-N	A6	Data2-	Data3+	B6	HB11-P
GND	A5			B5	GND
HB10-P	A4	Data2+	Data3-	B4	HB11-N
HB08-N	A3	Data0-	Data1+	B3	HB09-P
GND	A2			B2	GND
HB08-P	A1	Data0+	Data1-	B1	HB09-N

J17

Assigned	Pin	Signal	Signal	Pin	Assigned
(HB17-N - R44)++	A15	CLK-			
GND	A14				
(HB17-P - R45)++	A13	CLK+			
LA32-N	A12	Data6-	Data7+	B12	**LA33-P**
GND	A11			B11	GND
LA32-P	A10	Data6+	Data7-	B10	**LA33-N**
HB20-N	A9	Data4-	Data5+	B9	HB21-P
GND	A8			B8	GND
HB20-P	A7	Data4+	Data5-	B7	HB21-N
HB18-N	A6	Data2-	Data3+	B6	HB19-P
GND	A5			B5	GND
HB18-P	A4	Data2+	Data3-	B4	HB19-N
HB16-N	A3	Data0-	Data1+	B3	HB17-P
GND	A2			B2	GND
HB16-P	A1	Data0+	Data1-	B1	HB17-N

Vita57.1 Power Supply rails

Voltage supply	Voltage	Max. Current HPC (LPC)	Description
VADJ	0- 3.3V	4A (2A)	Adjustable supply voltage from CC to the IO MC module.
VIO-B-M2C	0 - VADJ	1.15 (NA)	Supplied voltage generated by MC powering the IO banks on the FPGA interfacing to the Bank B IO pins of the connector
VREF-A-M2C	0 - VADJ	1mA*	Reference voltage used by the bank A data pins, LAxx, HAxx. No Connect if Bank A reference voltage is not required.
VREF-B-M2C	0 - VIO-B-M2C	1mA (NA)*	Reference voltage used by the bank B data pins, HBxx. No Connect if Bank A reference voltage is not required.
3P3VAUX	3.3V	20mA*	Auxiliary power supply from CC to the IO MC module.
3P3	3.3V	3A	Power supply from CC to the IO MC module.
12P0V	12.0V	1A	Power supply from CC to the IO MC module.

NA: Not available for LPC connector **CC:** Carrier Card (Host) **MC:** Mezzanine Card

***** Due to supply rail's max. current limitation, the onboard LED indicator is populated but the current limiting resistor is NOT populated.

J20

Assigned	Pin	Pin	Assigned
VIO-B-M2C	1	2	3P3
VREF-A-M2C	3	4	VADJ
VREF-B-M2C	5	6	3P3VAUX
GND	7	8	12P0V

J23

Assigned	Pin	Pin	Assigned
TDI	1	2	TDO
3P3VAUX	3	4	TCK
I2C-SCL	5	6	TRST-L
I2C-SDA	7	8	TMS

J21

Assigned	Pin	Pin	Assigned
PG-C2M	1	2	PG-M2C*

* 10 K Ω (R17) pullup resistor to 3P3 supply rail

J22

Assigned	Pin	Pin	Assigned
CLK-DIR*	1	2	GND**

* 10 K Ω Pullup resistor R15 to 3P3 supply rail

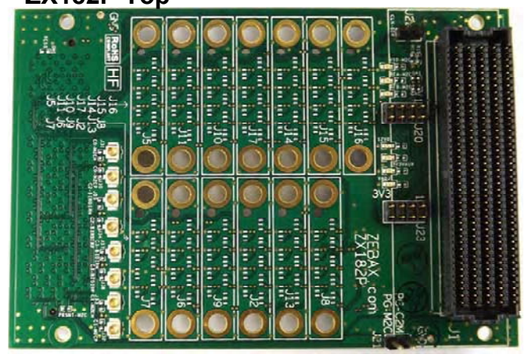
** 1M K Ω Pulldown resistor R16 to GND

NOTES:

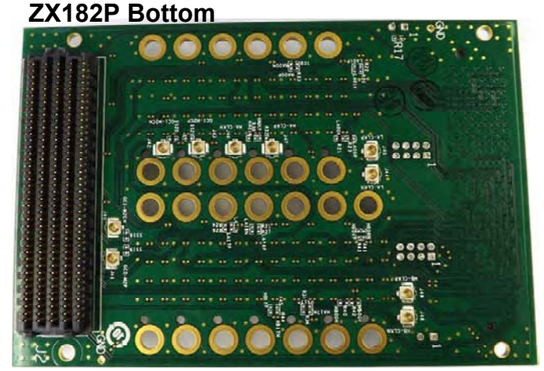
\+ IPEX connector access to the probe connector. The SSxx (0402 SMD package) enables MC Signal source. The SSxx Can be replaced by bead, ac coupling cap or filter.

++ Probe clock can be supplied from listed source, IPEX connector (if Jxx is listed) (X - Rx) and (Y-Ry) where X is the signal source followed by the enabled resistor, Rx. The Rx (0 Ω 0402 SMD package) must be installed in order to enable the signal as clock to the probe. Please see "Clock routing technique" section for more details.

ZX182P Top



ZX182P Bottom



Note

ALL ZEBAX products are **RoHS** compliant and **Lead Free** unless otherwise indicated.

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SPECIFIED DIMENSIONS ARE INCHES (MM). ROHS COMPLIANT

ASSEMBLY DRAWING

ITEM: ZX182P

DESCRIPTION: **FMC VITA 57.1 test board for P6880 Tektronix probe – passive mezzanine HPC LPC Meg-Array**

CHECKED: M. MARINA

DRAWN: SLAVIK

REVISSION: 1.0

SHEET: 3 OF 3