

Product Name: ZX182D FMC Vita 57.1 Tektronix D-MAX test board - breakout adapter passive FPGA Mezzanine Card
TekTronix – D-MAX probes P6980 P6982 differential probe or P6450 P6962 P6960HS

Product Description: FPGA Mezzanine card , FMC , passive breakout adapter, meeting VITA 57.1 standard bus interfacing with Tektronix D-Max differential / single ended probes, P6980 P6982. Includes 10 rows x 40 pins, totaling 400 pins High Pin Count, HPC, (200 pins for LPC – Low Pin Count), FCI Meg-Array, housing both CC (Carrier Card - Host) and MC (Mezzanine Card) connectors.

ZX182D is offered in HPC, LPC and FCI Meg-Array connector configuration, see ordering information

Fully compatible with 10 rows x 40 pins single ended or differential pairs design configuration

- All signals are accessible via designated probe's connector, IPEX, Header, and 0402 SMD package.
- All Clocks are accessible via IPEX-37 connectors
- JTAG signals accessible via 2x4 pin header
- All Power Supply signals accessible via 2x4 pin headers with on-board LEDs indicators.
- Improved signal integrity and crosstalk with **12 layers PCB** with each layers guarded by GROUND plane.
- Designed for **50Ω** single ended and **100Ω** differential trace impedance exceeding VITA 57.1 standard.
- DC to 10GHz bandwidth applications

GND test point for easy access as well as applying external ground reference

Application: FMC VITA 57.1 daughter card Bringup, testing, emulation, Xilinx development Virtex 6 Virtex 7 interface testing daughter board to host, modular design evaluations

Access: 2x4 pin header, SMD 0402 Package footprint as well as P68xx designated connectors

Pitch: 1.27mm (0.05") High Speed connector

Mates with : Xilinx FPGA development systems Virtex 6 Virtex 7 connecting daughter board to Host
 Any and all FMC VITA 57.1 compliant design CC-LPC-xxx CC-HPC-xxx MC-HPC-xxx MC-LPC-xxx where xxx is 10L, 10, 8.5L 8.5

Samtec Molex HI-SPEED HI-DENSITY SEARRAY design connectors.
 SEAM SADL SEAMP SEAR SEAMI SEAC FMC HPC LCP
 SEAF-040-08.0-L-10-2-A SEAF-040-08-L-10-2-A
 SEAFP-40 SEAMP-040 SEAMI-040 SEAR-040-10-10- SEAM-040
 All listed Samtec Molex FMC connectors listed, table below:

ZX18x FMC breakout adapter mates with the following Samtec Molex CC / MC SEARAY™ VITA 57.1 Connectors

Molex PN	Samtec PN	VITA PN	Description	Mated Stack Height
45971-4307	ASP-127796-01*	CC-LPC-10L	female	
45971-4317	ASP-134485-01*	CC-HPC-10L	female	
45971-4315	ASP-134486-01	CC-HPC-10	female	
45971-4305	ASP-134603-01	CC-LPC-10	female	
45970-4117	ASP-134601-01*	MC-HPC-8.5L	male	8.5 mm
45970-4115	ASP-134602-01	MC-HPC-8.5	male	8.5 mm
45970-4107	ASP-134605-01*	MC-LPC-8.5L	male	8.5 mm
45970-4105	ASP-134606-01	MC-LPC-8.5	male	8.5 mm
45970-4307	ASP-127797-01	MC-LPC-10L	male	10 mm
45970-4317	ASP-134487-01	MC-HPC-10L	male	10 mm
45970-4315	ASP-134488-01	MC-HPC-10	male	10 mm
45970-4305	ASP-134604-01	MC-LPC-10	male	10 mm

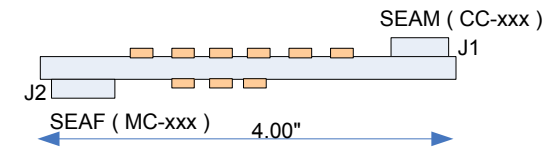
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ZX182D Block diagram, See Page 2

ZX182D , Passive FMC VITAL 57.1 breakout adapter – test board



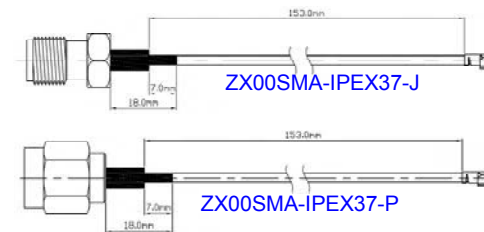
CC: Carrier Card typically located on Host
 MC: Mezzanine Card, typically located on Mezzanine Card
 SEAF: SEARRAY Female connector
 SEAM: SEARRAY Plug (Male) connector

Probe connector, headers, IPEX-37 access points

ZX182D-X-X Package includes:

Part number	Quantity	Description
ZX182D-X-X	1	FMC Mezzanine Module
ZX00SMA-IPEX37-X	4	SMA to IPEX-37 cable assembly , Note 1, See ordering information

Notes:
 1- Used for measuring or supplying external Clocks.



ZX182D-F-X Mates with any and all FMC VITA 57.1 compliant design using FCI Meg-Array 400 pins design. Meg-Array 10 rows x 40 pins FPGA Mezzanine Card (daughter)

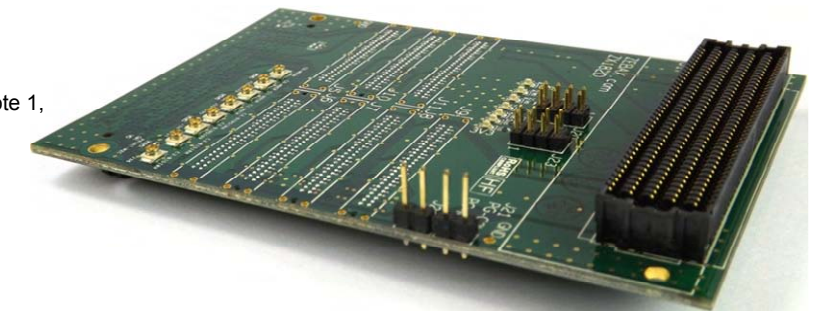
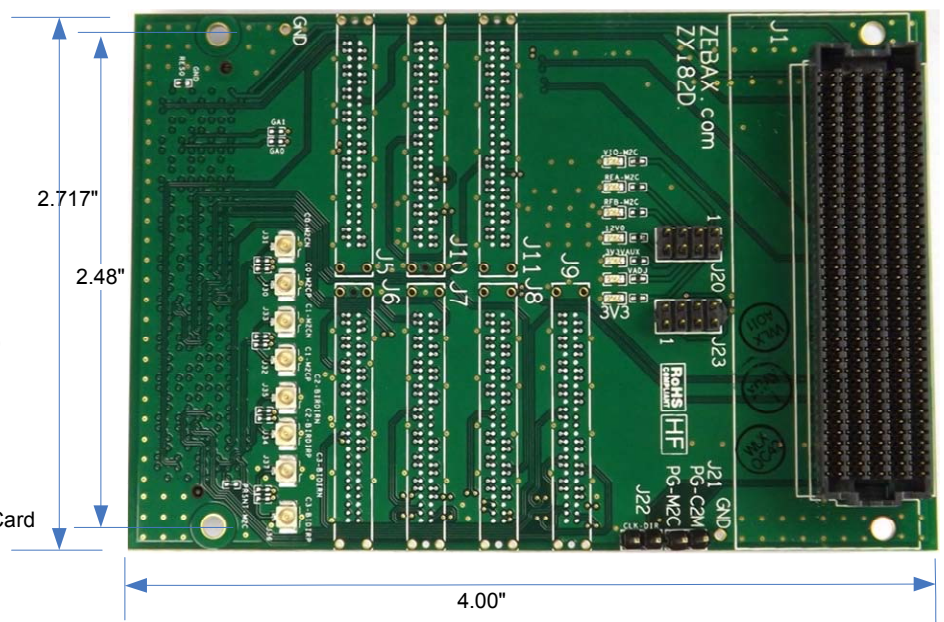
Mated Stack Height: 4mm 6mm 8mm 10mm 12mm 14mm
 Meets Telcordia GR-1217-CORE and NPS25298-2 Specifications

ZX18x-F-X FCI Meg-Array 10rows x 40 pins FMC breakout adapter mates with the following FCI Meg-Array VITA 57.1 Connectors

Plug (CC)		Receptacle (MC)		
84520-002LF	84740-002LF	74221-001LF	74388-001LF	74390-001LF*
84520-101LF	84740-102LF	74221-101LF	74388-101LF	74390-101LF
84520-202LF*	84740-202LF	74221-201LF	74388-201LF	74390-201LF
84520-092LF	84740-092LF	74221-091LF	74388-091LF	74390-091LF
84520-192LF	84740-192LF	74221-191LF	74388-191LF	74390-191LF
84520-292LF	84740-292LF	74221-291LF	74388-291LF	74390-201LF
6mm Plug	0mm Plug	4mm	6mm	8mm

* Used on ZX182P-F-X

LF : Lead Free



Ordering INFO:

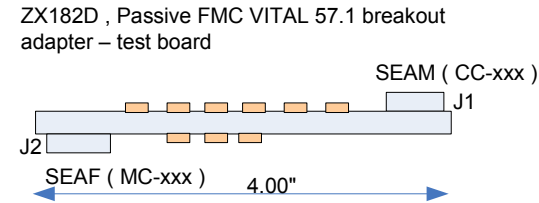
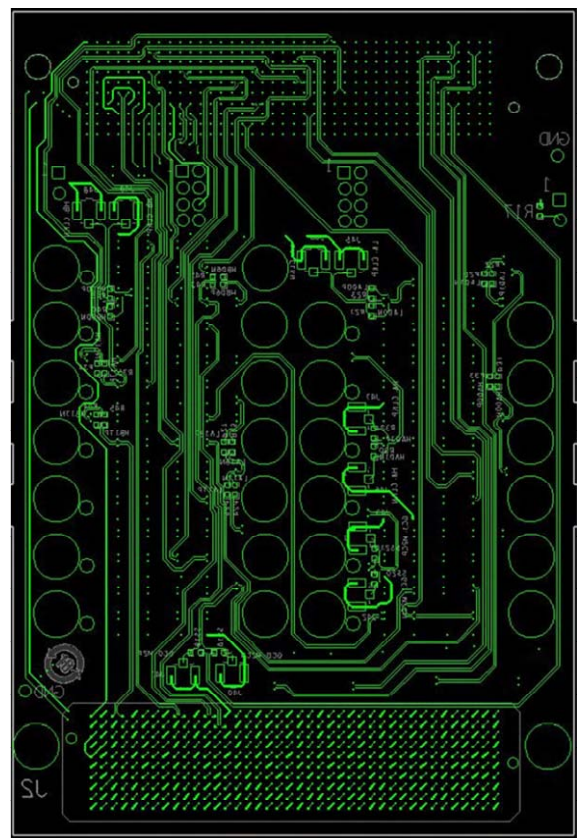
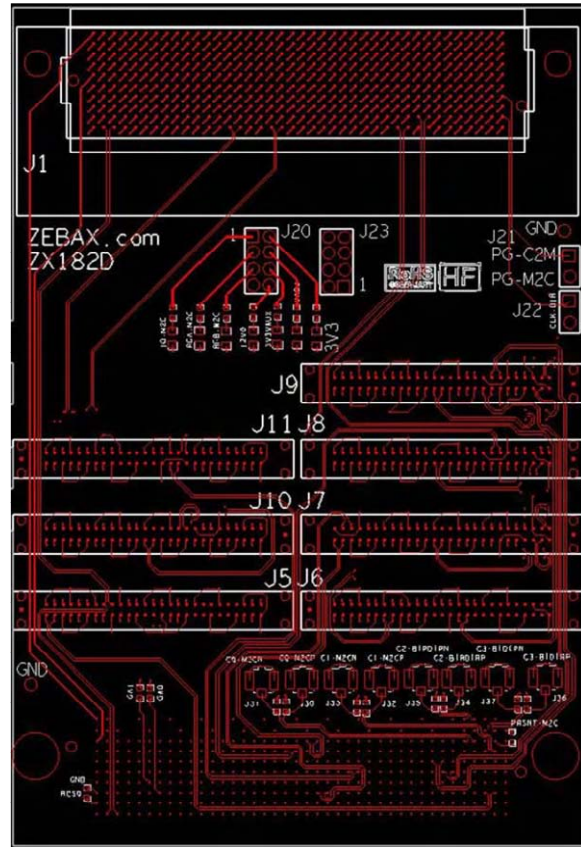
Part Number	options
ZX182D-X-X	J : SMA Jack (Standard) P : SMA Plug connector H : HPC - High Pin Count connector L : LPC - Low Pin Count connector F : FCI - FCI Meg-Array connector

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SPECIFIED DIMENSIONS ARE INCHES (MM). ROHS COMPLIANT	ASSEMBLY DRAWING ITEM: ZX182D
DESCRIPTION: FMC VITA 57.1 test board Tektronix D-MAX probe P6980 P6982 – passive mezzanine	
CHECKED: M. MARINA	DRAWN: SLAVIK
REVISION: 1.0 SHEET: 1 OF 3	

Product Name: ZX182D FMC Vita 57.1 Tektronix D-MAX P6980 P6982 test board - breakout adapter passive FPGA Mezzanine Card



ZX182D, Passive FMC VITAL 57.1 breakout adapter – test board

CC: Carrier Card typically located on Host
 MC: Mezzanine Card, typically located on Mezzanine Card
 SEAF: SEARRAY Female connector
 SEAM: SEARRAY Plug (Male) connector

Probe connector, headers, IPEX-37 access points

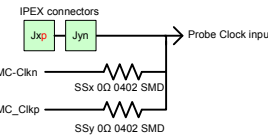
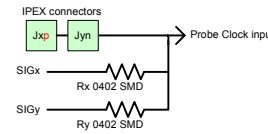
Typical SS signal connection using 0402 SMD Package

Break signal path:

Clock routing technique

Probe clocks are routed using IPEX connectors for use with external clock sources as well as optional resistor stuffing as exhibited below. Jxp, Jxn are IPEX positive and negative IPEX connectors. The Rx, Ry (0402 SMD package) are not stuffed as default. SIGx, SIGy are defined signals reserved as probe clock option, if available. Please see Probe signal assignment table for assigned IPEX and availability of SIGx, SIGy per designed probe access.

MC clock source routing to probes are accessible at IPEX connectors. SS (0402 SMD package) can be used to disconnect MC from providing the Clock or install appropriate filtering, if applicable.



Tektronix D-MAX probe P6890 P6892

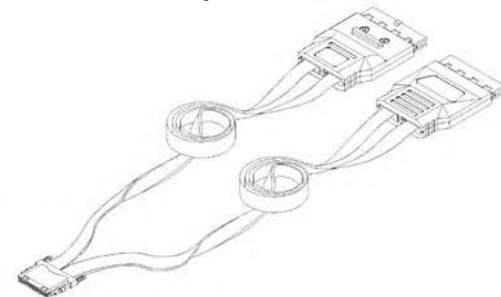
D-MAX probe technology is nonintrusive using compression Land Grid Array, cLGA, connector that provides electrical connection between PCB and the probe.

D-MAX probe can be installed to ZX182D using :

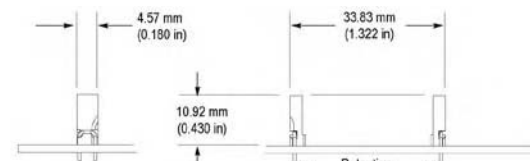
1- Probe retention posts Tektronix part number: **020-2539-00**

2- Alternate retention assembly – Tektronix part number: **020-2908-xx qty of 2**
020-2910-xx qty of 50

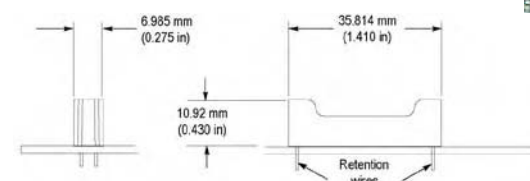
ZX182D does NOT contain the retention posts or the Alternate retention assembly.



Probe retention posts Tektronix part number: 020-2539-00

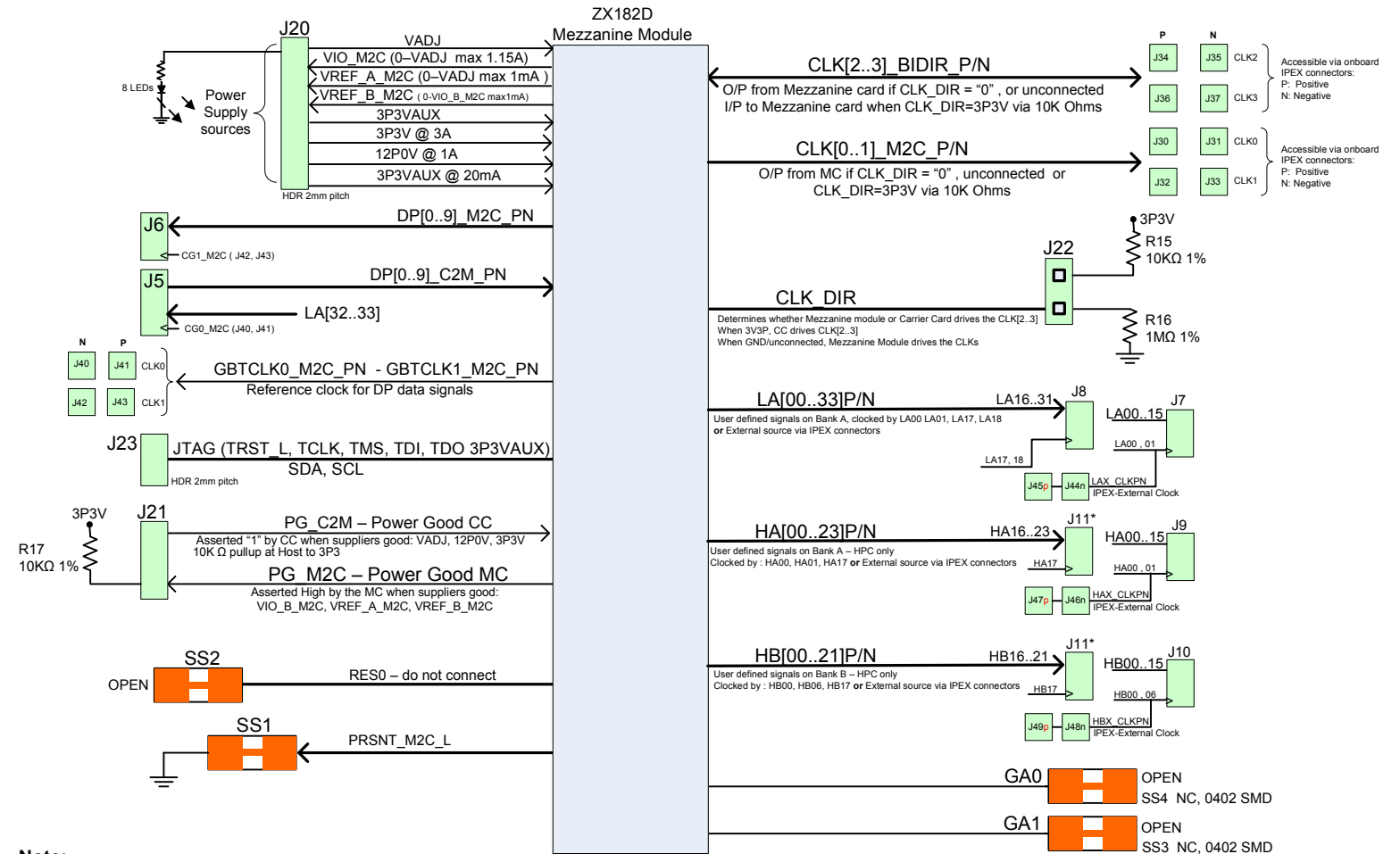


Alternate retention assembly – Tektronix part number: 020-2908-xx qty of 2
020-2910-xx qty of 50



Note:

- 1- MC Mezzanine Card - CC Carrier Card (Host)
- 2- All Clocks are accessible via onboard IPEX connectors
- 3- IPEX Jxpx is shared terminal, Jxnx is negative terminal of the external clock source.
- 4- J11* - J11 is shared connector supporting HA and HB signals. It has HA17 and HB17 clocking options



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ITEM: ZX182D		
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CHECKED: M. MARINA	DRAWN: SLAVIK	REVISION: 1.0
		SHEET: 2 OF 3

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Probe signal map: Below are signal and clock mapping for the designated P6980 P6982 probe connectors

J5						
Assigned	Pin	Signal	Signal	Pin	Assigned	
DP0-C2M-P	A1	D0+	GND	B1	GND	
DP0-C2M-N	A2	D0-	D1-	B2		DP1-C2M-N
	A3	GND	D1+	B3		DP1-C2M-P
DP2-C2M-P	A4	D2+	GND	B4	GND	
DP2-C2M-N	A5	D2-	D3-	B5		DP3-C2M-N
	A6	GND	D3+	B6		DP3-C2M-P
DP4-C2M-P	A7	D4+	GND	B7	GND	
DP4-C2M-N	A8	D4-	D5-	B8		DP5-C2M-N
	A9	GND	D5+	B9		DP5-C2M-P
DP6-C2M-P	A10	D6+	GND	B10	GND	
DP6-C2M-N	A11	D6-	D7-	B11		DP7-C2M-N
	A12	GND	D7+	B12		DP7-C2M-P
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	GBTCLK0-M2C-N J40 - SS18
	GND	A15	GND	CLK+	B15	GBTCLK0-M2C-P J41 - SS19
DP8-C2M-P	A16	D8+	GND	B16	GND	
DP8-C2M-N	A17	D8-	D9-	B17		DP9-C2M-N
	A18	GND	D9+	B18		DP9-C2M-P
NC	A19	D10+	GND	B19	GND	
NC	A20	D10-	D11-	B20	NC	
	GND	A21	GND	D11+	B21	NC
NC	A22	D12+	GND	B22	GND	
NC	A23	D12-	D13-	B23	NC	
	GND	A24	GND	D13+	B24	NC
LA32-P	A25	D14+	GND	B25	GND	
LA32-N	A26	D14-	D15-	B26		LA33-P
	GND	A27	GND	D15+	B27	

J11						
Assigned	Pin	Signal	Signal	Pin	Assigned	
HB16-P	A1	D0+	GND	B1	GND	
HB16-N	A2	D0-	D1-	B2		HB17-N
	A3	GND	D1+	B3		HB17-P
HB18-P	A4	D2+	GND	B4	GND	
HB18-N	A5	D2-	D3-	B5		HB19-N
	A6	GND	D3+	B6		HB19-P
HB20-P	A7	D4+	GND	B7	GND	
HB20-N	A8	D4-	D5-	B8		HB21-N
	A9	GND	D5+	B9		HB21-P
NC	A10	D6+	GND	B10	GND	
NC	A11	D6-	D7-	B11	NC	
	GND	A12	GND	D7+	B12	NC
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	HB17-N - R44 HA17-N - R45
	GND	A15	GND	CLK+	B15	HB17-P - R46 HA17-P - R47
HA16-P	A16	D8+	GND	B16	GND	
HA16-N	A17	D8-	D9-	B17		HA17-N
	A18	GND	D9+	B18		HA17-P
HA18-P	A19	D10+	GND	B19	GND	
HA18-N	A20	D10-	D11-	B20		HA19-N
	GND	A21	GND	D11+	B21	HA19-P
HA20-P	A22	D12+	GND	B22	GND	
HA20-N	A23	D12-	D13-	B23		HA21-N
	GND	A24	GND	D13+	B24	HA21-P
HA22-P	A25	D14+	GND	B25	GND	
HA22-N	A26	D14-	D15-	B26		HA23-N
	GND	A27	GND	D15+	B27	HA23-P

J8						
Assigned	Pin	Signal	Signal	Pin	Assigned	
LA16-P	A1	D0+	GND	B1	GND	
LA16-N	A2	D0-	D1-	B2		LA17-N
	A3	GND	D1+	B3		LA17-P
LA18-P	A4	D2+	GND	B4	GND	
LA18-N	A5	D2-	D3-	B5		LA19-N
	A6	GND	D3+	B6		LA19-P
LA20-P	A7	D4+	GND	B7	GND	
LA20-N	A8	D4-	D5-	B8		LA21-N
	A9	GND	D5+	B9		LA21-P
LA22-P	A10	D6+	GND	B10	GND	
LA22-N	A11	D6-	D7-	B11		LA23-N
	GND	A12	GND	D7+	B12	LA23-P
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	LA17-N - R24 LA18-N - R25
	GND	A15	GND	CLK+	B15	LA17-P - R26 LA18-P - R27
LA24-P	A16	D8+	GND	B16	GND	
LA24-N	A17	D8-	D9-	B17		LA25-N
	A18	GND	D9+	B18		LA25-P
LA26-P	A19	D10+	GND	B19	GND	
LA26-N	A20	D10-	D11-	B20		LA27-N
	GND	A21	GND	D11+	B21	LA27-P
LA28-P	A22	D12+	GND	B22	GND	
LA28-N	A23	D12-	D13-	B23		LA29-N
	GND	A24	GND	D13+	B24	LA29-P
LA30-P	A25	D14+	GND	B25	GND	
LA30-N	A26	D14-	D15-	B26		LA31-N
	GND	A27	GND	D15+	B27	LA31-P

Vita57.1 Power Supply rails				
Voltage supply	Voltage	Max. Current HPC (LPC)	Description	
VADJ	0- 3.3V	4A (2A)	Adjustable supply voltage from CC to the IO MC module.	
VIO-B-M2C	0 - VADJ	1.15 (NA)	Supplied voltage generated by MC powering the IO banks on the FPGA interfacing to the Bank B IO pins of the connector	
VREF-A-M2C	0 - VADJ	1mA*	Reference voltage used by the bank A data pins, LAXx, HAXx. No Connect if Bank A reference voltage is not required.	
VREF-B-M2C	0 - VIO-B-M2C	1mA (NA)*	Reference voltage used by the bank B data pins, HBxx. No Connect if Bank A reference voltage is not required.	
3P3VAUX	3.3V	20mA*	Auxiliary power supply from CC to the IO MC module.	
3P3	3.3V	3A	Power supply from CC to the IO MC module.	
12P0V	12.0V	1A	Power supply from CC to the IO MC module.	

NA: Not available for LPC connector CC: Carrier Card (Host) MC: Mezzanine Card
* Due to supply rail's max. current limitation, the onboard LED indicator is populated but the current limiting resistor is NOT populated.

J6						
Assigned	Pin	Signal	Signal	Pin	Assigned	
DP0-M2C-P	A1	D0+	GND	B1	GND	
DP0-M2C-N	A2	D0-	D1-	B2		DP1-M2C-N
	A3	GND	D1+	B3		DP1-M2C-P
DP2-M2C-P	A4	D2+	GND	B4	GND	
DP2-M2C-N	A5	D2-	D3-	B5		DP3-M2C-N
	A6	GND	D3+	B6		DP3-M2C-P
DP4-M2C-P	A7	D4+	GND	B7	GND	
DP4-M2C-N	A8	D4-	D5-	B8		DP5-M2C-N
	A9	GND	D5+	B9		DP5-M2C-P
DP6-M2C-P	A10	D6+	GND	B10	GND	
DP6-M2C-N	A11	D6-	D7-	B11		DP7-M2C-N
	A12	GND	D7+	B12		DP7-M2C-P
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	GBTCLK1-M2C-N J42 - SS20
	GND	A15	GND	CLK+	B15	GBTCLK1-M2C-P J43 - SS21
DP8-M2C-P	A16	D8+	GND	B16	GND	
DP8-M2C-N	A17	D8-	D9-	B17		DP9-M2C-N
	A18	GND	D9+	B18		DP9-M2C-P
NC	A19	D10+	GND	B19	GND	
NC	A20	D10-	D11-	B20	NC	
	GND	A21	GND	D11+	B21	NC
NC	A22	D12+	GND	B22	GND	
NC	A23	D12-	D13-	B23	NC	
	GND	A24	GND	D13+	B24	NC
NC	A25	D14+	GND	B25	GND	
NC	A26	D14-	D15-	B26	NC	
	GND	A27	GND	D15+	B27	NC

J9						
Assigned	Pin	Signal	Signal	Pin	Assigned	
HA00-P	A1	D0+	GND	B1	GND	
HA00-N	A2	D0-	D1-	B2		HA01-N
	A3	GND	D1+	B3		HA01-P
HA02-P	A4	D2+	GND	B4	GND	
HA02-N	A5	D2-	D3-	B5		HA03-N
	A6	GND	D3+	B6		HA03-P
HA04-P	A7	D4+	GND	B7	GND	
HA04-N	A8	D4-	D5-	B8		HA05-N
	A9	GND	D5+	B9		HA05-P
HA06-P	A10	D6+	GND	B10	GND	
HA06-N	A11	D6-	D7-	B11		HA07-N
	GND	A12	GND	D7+	B12	HA07-P
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	XHA-CLKN - J46 HA00-N - R30 HA01-N - R31 XHA-CLKP - J47 HA00-P - R32 HA01-N - R33
HA08-P	A16	D8+	GND	B16	GND	
HA08-N	A17	D8-	D9-	B17		HA09-N
	A18	GND	D9+	B18		HA09-P
HA10-P	A19	D10+	GND	B19	GND	
HA10-N	A20	D10-	D11-	B20		HA11-N
	GND	A21	GND	D11+	B21	HA11-P
HA12-P	A22	D12+	GND	B22	GND	
HA12-N	A23	D12-	D13-	B23		HA13-N
	GND	A24	GND	D13+	B24	HA13-P
HA14-P	A25	D14+	GND	B25	GND	
HA14-N	A26	D14-	D15-	B26		HA15-N
	GND	A27	GND	D15+	B27	HA15-P

J7						
Assigned	Pin	Signal	Signal	Pin	Assigned	
LA00-P	A1	D0+	GND	B1	GND	
LA00-N	A2	D0-	D1-	B2		LA01-N
	A3	GND	D1+	B3		LA01-P
LA02-P	A4	D2+	GND	B4	GND	
LA02-N	A5	D2-	D3-	B5		LA03-N
	A6	GND	D3+	B6		LA03-P
LA04-P	A7	D4+	GND	B7	GND	
LA04-N	A8	D4-	D5-	B8		LA05-N
	A9	GND	D5+	B9		LA05-P
LA06-P	A10	D6+	GND	B10	GND	
LA06-N	A11	D6-	D7-	B11		LA07-N
	GND	A12	GND	D7+	B12	LA07-P
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	XLA-CLKN - J44 LA00-N - R20 LA01-N - R21
	GND	A15	GND	CLK+	B15	XLA-CLKP - J45 LA00-P - R22 LA01-P - R23
LA08-P	A16	D8+	GND	B16	GND	
LA08-N	A17	D8-	D9-	B17		LA09-N
	A18	GND	D9+	B18		LA09-P
LA10-P	A19	D10+	GND	B19	GND	
LA10-N	A20	D10-	D11-	B20		LA11-N
	GND	A21	GND	D11+	B21	LA11-P
LA12-P	A22	D12+	GND	B22	GND	
LA12-N	A23	D12-	D13-	B23		LA13-N
	GND	A24	GND	D13+	B24	LA13-P
LA14-P	A25	D14+	GND	B25	GND	
LA14-N	A26	D14-	D15-	B26		LA15-N
	GND	A27	GND	D15+	B27	LA15-P

J10						
Assigned	Pin	Signal	Signal	Pin	Assigned	
HB00-P	A1	D0+	GND	B1	GND	
HB00-N	A2	D0-	D1-	B2		HB01-N
	A3	GND	D1+	B3		HB01-P
HB02-P	A4	D2+	GND	B4	GND	
HB02-N	A5	D2-	D3-	B5		HB03-N
	A6	GND	D3+	B6		HB03-P
HB04-P	A7	D4+	GND	B7	GND	
HB04-N	A8	D4-	D5-	B8		HB05-N
	A9	GND	D5+	B9		HB05-P
HB06-P	A10	D6+	GND	B10	GND	
HB06-N	A11	D6-	D7-	B11		HB07-N
	GND	A12	GND	D7+	B12	HB07-P
NC	A13	NC	GND	B13	GND	
	NC	A14	NC	CLK-	B14	XHB-CLKN - J46 HB00-N - R40 HB06-N - R41
	GND	A15	GND	CLK+	B15	XHB-CLKP - J49 HB00-P - R42 HB06-P - R43
HB08-P	A16	D8+	GND	B16	GND	
HB08-N	A17	D8-	D9-	B17		HB09-N