

Product Name: ZX149-QTE 060 FPGA Xilinx Virtex Breakout Adapter

Product Description: QTE-060 60x2, 120 pins Samtec breakout adapter supporting Samtec's HI-SPEED Header Q-Strip Blade & Beam Design connectors.

Fully compatible with HITECHGLOBAL, HTG-V6-PCIE Virtec 6 FPGA development solutions

- Designed for characterization, timing analysis, bringup and testing of FPGA solutions with **90Ω differential pair signal impedance**
- Designed for use with Agilent **E5381A** differential probe or similar using multiple probes.
- Designed in 4 layer PCBoard
- No via on any signal traces
- Improved signal integrity and crosstalk.
- Matching connector's 8GHz bandwidth applications

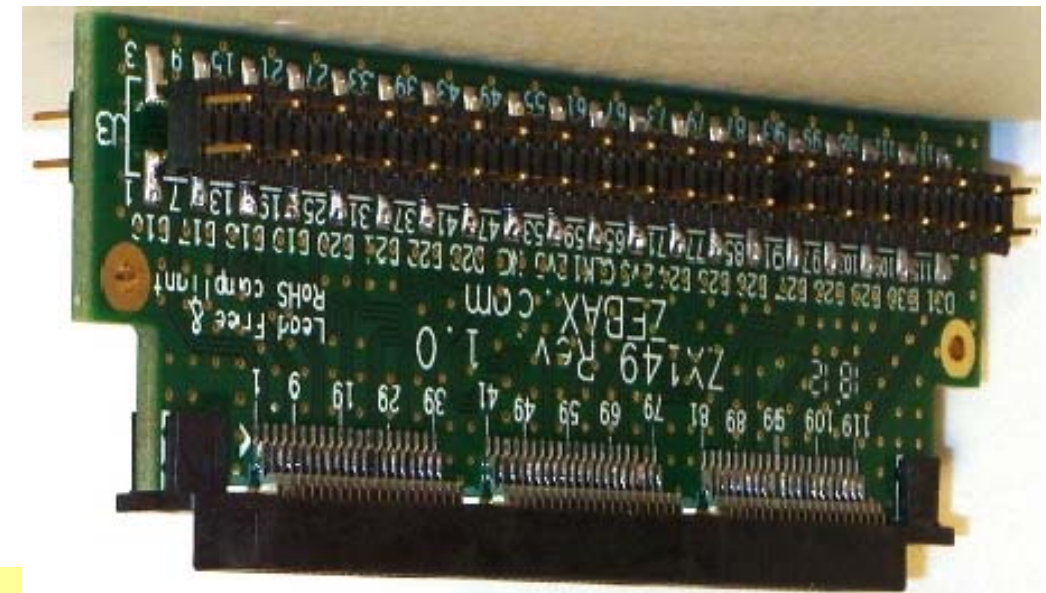
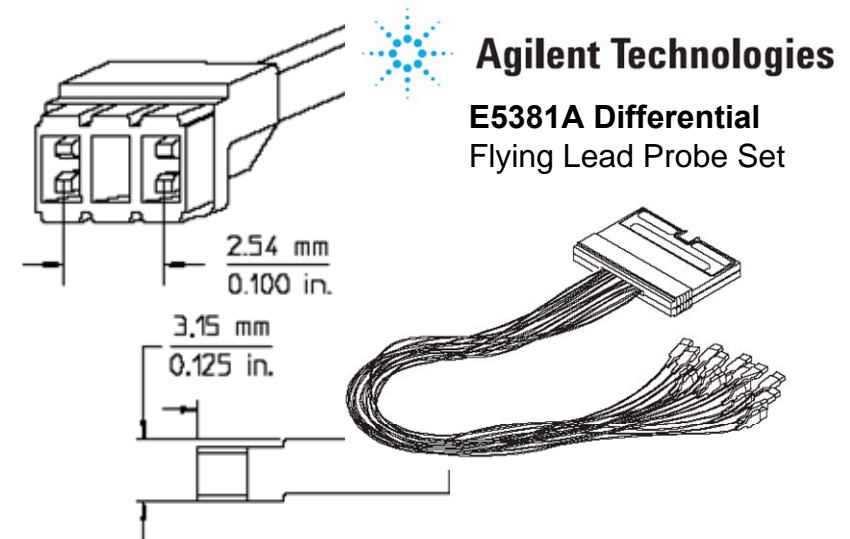
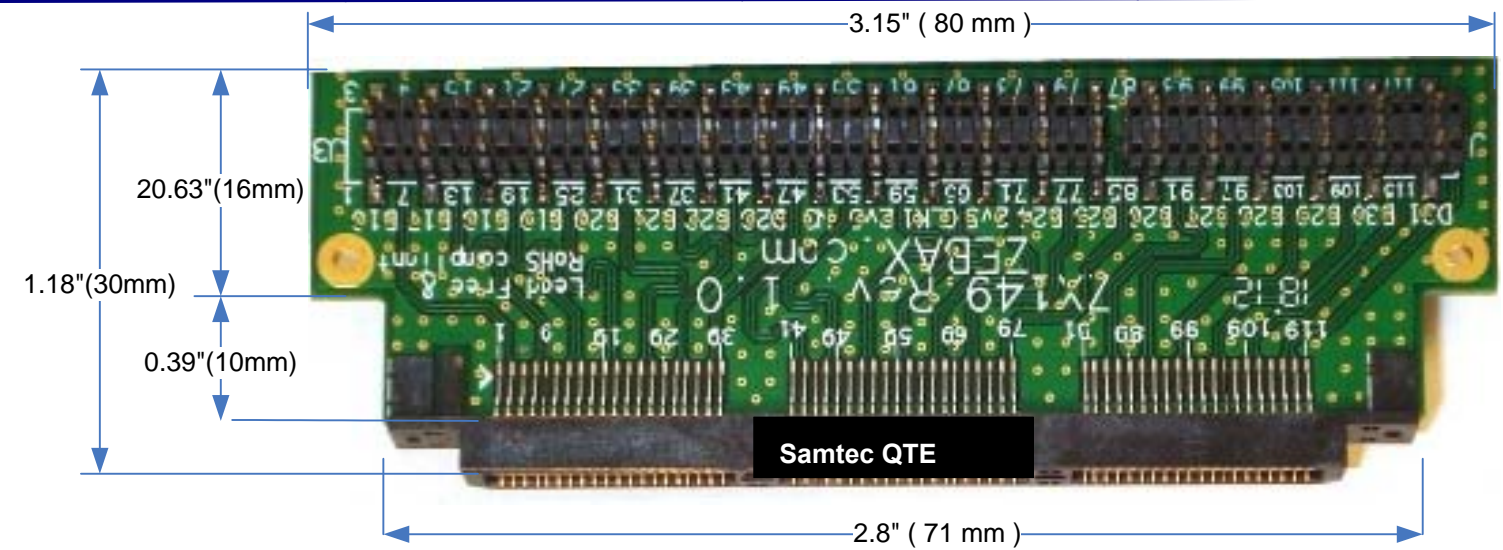
GND test point for easy access

Application: Timing analysis, Bringup, characterization, testing, emulation, development, modular design evaluations

Mates with : Samtec QSE-060-L-D QSE-042-01-DP connectors and any **3 banks** of QSE-080 (-056 Differential pair, -DP) Agilent E5381A differential probe or similar using multiple probes.

Pitch: **Samtec** 0.80mm (0.0315") High Speed connector

Headers: Pin Center - 0.1" (2.54mm)
Pitch - 0.15" (4mm)
Pin diameter - 0.018" (0.46mm)
Post height - 0.157 (4mm)
Meeting differential probe Agilent E5381A or similar.



ZX149-QTE060 pin configuration

TOP	QTE	J1	LVDS00N																			
BOTTOM			LVDS00P																			
Layer			LVDS16_N																			
Bottom	Headers	J4-J5	4	10	16	22	28	34	40	44	50	56	62	68	74	80	88	94	100	106	112	118
			2	8	14	20	26	32	38	42	48	54	60	66	72	78	86	92	98	104	110	116
			LVDS00P	LVDS01	LVDS02	LVDS03	LVDS04	LVDS05	LVDS06	LVDS07	RES2	3.3V	DIFFCLK-0	3.3V	LVDS08	LVDS09	LVDS10	LVDS11	LVDS12	LVDS13	LVDS14	LVDS15
			LVDS16_N																			
Top	Headers	J2-J3	3	9	15	21	27	33	39	43	49	55	61	67	73	79	87	93	99	105	111	117
			1	7	13	19	25	31	37	41	47	53	59	65	71	77	85	91	97	103	109	115
			LVDS16_P	LVDS17	LVDS18	LVDS19	LVDS20	LVDS21	LVDS22	LVDS23	RES1	2.5V	DIFFCLK-1	2.5V	LVDS24	LVDS25	LVDS26	LVDS27	LVDS28	LVDS29	LVDS30	LVDS31

- Note
- 1- Labeled header pin numbers refer to Samtec QTE connector pin
 - 2- Headers top row are assigned to xxxx_N, negative whereas the bottom rows are assigned to xxx_P positive signal pair of differential signal pair.
 - 3- RES1, RES2 signal pairs are user dependent as not assigned by Target system
 - 4- Unmarked pins are connected to GROUND - The GND test point (TP) must be used for any GND reference.
 - 5- Connector's GND center tap has mechanical contact with board's GND plane.
 - 6- Differential pairs labeled **3.3V** (54-56, 66-68) , **2.5V** (53-55, 65-67) **are labeled to match** assigned voltage rails on HITECHGLOBAL, HTG-V6-PCIE connector interface. Other users may use these signals pairs as another differential / single pair.

ALL ZEBAX products are RoHS compliant and Lead Free unless otherwise indicated.

Notice
ALL ZEBAX TECHNOLOGIES DESIGN SPECIFICATIONS, DRAWINGS, PUBLICATIONS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." ZEBAX MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NO INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE.
Information furnished is believed to be accurate and reliable. However, Zebax Technologies assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use. Specifications mentioned in this publication are subject to change without notice. This publication replaces all other information previously supplied. Zebax Technologies products are not authorized as in life support devices or systems.

ZEBAX TECHNOLOGIES
SANTA CRUZ, CA U.S.A (831) 222-0717
WWW.ZEBAX.COM

SPECIFIED DIMENSIONS ARE INCHES (MM). ROHS COMPLIANT	ASSEMBLY DRAWING	
	ITEM: ZX149 FPGA Xilinx Virtex	
DESCRIPTION: ZX149-QTE 060 FPGA Xilinx Virtex Breakout Adapter		
CHECKED: M. MARINA	DRAWN: SLAVIK	REVISION: 1.0
		SHEET: 1 OF 1